

	Hits	Search Text	Dbs	Time Stamp
1	6664	707/1-4,7,8,10.ccls.	USPAT	2003/10/07 15:17
2	4435	707/100-102,104.1.ccls.	USPAT	2003/10/07 15:17
3	3234	707/200-206.ccls.	USPAT	2003/10/07 15:18
4	3660	711/1,100-104,111-113,115.ccls .	USPAT	2003/10/02 10:51
5	3942	365/175.01,185.18,185.29,185.3 3,189.01,218.ccls.	USPAT	2003/10/02 10:53
6	1366	713/1,2.ccls.	USPAT	2003/10/02 10:53
7	3638	235/375,380,382.ccls.	USPAT	2003/10/02 10:54
8	1534	710/1,3,8,13.ccls.	USPAT	2003/10/02 10:54
9	10667	707/1-4,7,8,10.ccls. or 707/100-102,104.1.ccls. or 707/200-206.ccls.	USPAT	2003/10/06 14:10
10	10326	235/375,380,382.ccls. or 365/175.01,185.18,185.29,185.3 3,189.01,218.ccls. or 710/1,3,8,13.ccls. or 713/1,2.ccls.	USPAT	2003/10/03 08:27
11	10667	707/1-4,7,8,10.ccls. or 707/100-102,104.1.ccls. or 707/200-206.ccls.	USPAT	2003/10/09 09:52
12	10326	235/375,380,382.ccls. or 365/175.01,185.18,185.29,185.3 3,189.01,218.ccls. or 710/1,3,8,13.ccls. or 713/1,2.ccls.	USPAT	2003/10/09 09:53
13	3966	(ic or (integrated adj circuit)) and processor\$2 and (volatile adj2 memory) and (non\$2volatile adj2 memory)	USPAT	2003/10/03 11:13
14	1272	(file adj system) and (manag\$4 with access) and (stor\$4 with memory)	USPAT	2003/10/03 10:34
15	48	(file adj system) and (manag\$4 with access) and (stor\$4 with memory) and ((ic or (integrated adj circuit)) and processor\$2 and (volatile adj2 memory) and (non\$2volatile adj2 memory))	USPAT	2003/10/03 08:31

	Hits	Search Text	DBs	Time Stamp
16	9	((707/1-4,7,8,10.ccls. or 707/100-102,104.1.ccls. or 707/200-206.ccls.) or (235/375,380,382.ccls. or 365/175.01,185.18,185.29,185.33,189.01,218.ccls. or 710/1,3,8,13.ccls. or 713/1,2.ccls.)) and ((file adj system) and (manag\$4 with access) and (stor\$4 with memory) and ((ic or (integrated adj circuit)) and processor\$2 and (volatile adj2 memory) and (non\$2volatile adj2 memory)))	USPAT	2003/10/03 10:31
17	1648	(application adj program adj interface\$2) and function\$2 and parameter\$2	USPAT	2003/10/03 10:38
18	1272	(file adj system) and (manag\$4 with access) and (stor\$4 with memory) and ((file adj system) and (manag\$4 with access) and (stor\$4 with memory))	USPAT	2003/10/03 10:35
19	48	(file adj system) and (manag\$4 with access) and (stor\$4 with memory) and ((file adj system) and (manag\$4 with access) and (stor\$4 with memory)) and ((ic or (integrated adj circuit)) and processor\$2 and (volatile adj2 memory) and (non\$2volatile adj2 memory))	USPAT	2003/10/03 10:35
20	146	(application adj program adj interface\$2) and function\$2 and parameter\$2 and ((file adj system) and (manag\$4 with access) and (stor\$4 with memory) and ((file adj system) and (manag\$4 with access) and (stor\$4 with memory)))	USPAT	2003/10/03 11:14
21	13	(application adj program adj interface\$2) and function\$2 and parameter\$2 and ((file adj system) and (manag\$4 with access) and (stor\$4 with memory) and ((file adj system) and (manag\$4 with access) and (stor\$4 with memory))) and ((ic or (integrated adj circuit)) and processor\$2 and (volatile adj2 memory) and (non\$2volatile adj2 memory))	USPAT	2003/10/03 10:39
22	25120	(volatile adj2 memory) and (non\$2volatile adj2 memory)	USPAT	2003/10/03 11:13

	Hits	Search Text	DBs	Time Stamp
23	24	(application adj program adj interface\$2) and function\$2 and parameter\$2 and ((file adj system) and (manag\$4 with access) and (stor\$4 with memory) and ((file adj system) and (manag\$4 with access) and (stor\$4 with memory))) and ((volatile adj2 memory) and (non\$2volatile adj2 memory))	USPAT	2003/10/06 15:43
24	10667	707/1-4,7,8,10.ccls. or 707/100-102,104.1.ccls. or 707/200-206.ccls.	USPAT	2003/10/06 14:10
25	10326	235/375,380,382.ccls. or 365/175.01,185.18,185.29,185.3 3,189.01,218.ccls. or 710/1,3,8,13.ccls. or 713/1,2.ccls.	USPAT	2003/10/06 14:10
26	30	(smart adj card) and (manag\$4 with access) and (stor\$4 with memory) and ((volatile adj2 memory) and (non\$2volatile adj2 memory)) and computer and (file adj system\$2)	USPAT	2003/10/06 15:45
27	94	(smart adj card) and (manag\$4 with access) and (stor\$4 with memory) and ((volatile adj2 memory) and (non\$2volatile adj2 memory))	USPAT	2003/10/07 08:33
28	6686	707/1-4,7,8,10.ccls.	USPAT	2003/10/07 07:38
29	4452	707/100-102,104.1.ccls.	USPAT	2003/10/07 07:38
30	3242	707/200-206.ccls.	USPAT	2003/10/07 07:38
31	10704	707/1-4,7,8,10.ccls. or 707/100-102,104.1.ccls. or 707/200-206.ccls.	USPAT	2003/10/07 07:38
32	10338	235/375,380,382.ccls. or 365/175.01,185.18,185.29,185.3 3,189.01,218.ccls. or 710/1,3,8,13.ccls. or 713/1,2.ccls.	USPAT	2003/10/07 07:39
33	7486	((identif\$4 or indicat\$4 or determin\$4) with stor\$4 with memory) and ((volatile adj2 memory) and (non\$2volatile adj2 memory))	USPAT	2003/10/07 08:35

	Hits	Search Text	DBs	Time Stamp
34	953	((707/1-4,7,8,10.ccls. or 707/100-102,104.1.ccls. or 707/200-206.ccls.) or (235/375,380,382.ccls. or 365/175.01,185.18,185.29,185.3 3,189.01,218.ccls. or 710/1,3,8,13.ccls. or 713/1,2.ccls.)) and (((identif\$4 or indicat\$4 or determin\$4) with stor\$4 with memory) and ((volatile adj2 memory) and (non\$2volatile adj2 memory)))	USPAT	2003/10/07 08:36
35	231	((707/1-4,7,8,10.ccls. or 707/100-102,104.1.ccls. or 707/200-206.ccls.) or (235/375,380,382.ccls. or 365/175.01,185.18,185.29,185.3 3,189.01,218.ccls. or 710/1,3,8,13.ccls. or 713/1,2.ccls.)) and (((identif\$4 or indicat\$4 or determin\$4) with stor\$4 with volatile adj2 memory) and (non\$2volatile adj2 memory))	USPAT	2003/10/07 08:38
36	215	((707/1-4,7,8,10.ccls. or 707/100-102,104.1.ccls. or 707/200-206.ccls.) or (235/375,380,382.ccls. or 365/175.01,185.18,185.29,185.3 3,189.01,218.ccls. or 710/1,3,8,13.ccls. or 713/1,2.ccls.)) and (((identif\$4 or indicat\$4 or determin\$4) with stor\$4 with volatile adj memory) and (non\$2volatile adj2 memory))	USPAT	2003/10/07 08:39
37	6686	707/1-4,7,8,10.ccls.	USPAT	2003/10/07 15:17
38	4452	707/100-102,104.1.ccls.	USPAT	2003/10/07 15:18
39	3242	707/200-206.ccls.	USPAT	2003/10/07 15:18
40	10704	707/1-4,7,8,10.ccls. or 707/100-102,104.1.ccls. or 707/200-206.ccls.	USPAT	2003/10/07 15:18
41	10338	235/375,380,382.ccls. or 365/175.01,185.18,185.29,185.3 3,189.01,218.ccls. or 710/1,3,8,13.ccls. or 713/1,2.ccls.	USPAT	2003/10/07 15:18
42	10704	707/1-4,7,8,10.ccls. or 707/100-102,104.1.ccls. or 707/200-206.ccls.	USPAT	2003/10/09 09:52

	Hits	Search Text	DBs	Time Stamp
43	10338	235/375,380,382.ccls. or 365/175.01,185.18,185.29,185.3 3,189.01,218.ccls. or 710/1,3,8,13.ccls. or 713/1,2.ccls.	USPAT	2003/10/09 09:53

File 348:EUROPEAN PATENTS 1978-2003/Mar W05
(c) 2003 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20030403,UT=20030327
(c) 2003 WIPO/Univentio
? ds

Set	Items	Description
S1	83025	(SMART OR CHIP OR STORED OR CRYPTO OR ACCESS OR SECURITY OR VALUE OR TRANSACTION? ? OR IC OR PAYMENT? ? OR PROGRAMMABLE)-(2W)CARD?? OR INTEGRATED()CIRCUIT? ? OR ELECTRONIC(1W)(PURSE?? OR WALLET?? OR CARD? ?)
S2	20817	(VOLATILE OR UNSTABLE OR NONPERSISTENT OR NON()PERSISTENT - OR TRANSIENT)(3N)(STOR???? OR MEMOR???)
S3	89314	RAM OR RANDOM()ACCESS()MEMORY OR DRAM OR SRAM OR SDRAM OR RDRAM OR SLDRAM OR SGRAM OR DRDRAM
S4	14131	(NONVOLATILE OR "NON-VOLATILE" OR PERSISTENT OR PERMANENT)-(3N)(STOR? OR MEMOR???)
S5	120097	ROM OR READ()ONLY()MEMORY OR PROM OR EPROM OR EEPROM
S6	24710	(S2:S5 OR MEMOR???) (5N) (FILE? ? OR OBJECT? ? OR DOCUMENT? ? OR CONTENT)
S7	126318	(ACCESS? OR RETRIEV? OR OBTAIN? OR FIND??? OR SEARCH??? OR TRACK???) (5N) (FILE? ? OR OBJECT? ? OR DOCUMENT? ? OR CONTENT)
S8	116765	(TABLE? ? OR DIRECTOR??? OR REPOSITOR??? OR DATABASE? ? OR DATA()BASE? ? OR LIST???) (5N) (FILE? ? OR OBJECT? ? OR DOCUMENT? ? OR CONTENT)
S9	37988	(AUTHORIZ? OR AUTHORIZ? OR CLEAR? OR CREDENTIAL? ? OR PERMISSION? ? OR PERMIT? OR ALLOW?) (5N) (FILE? ? OR OBJECT? ? OR DOCUMENT? ? OR CONTENT)
S10	13415	APPLICATION()PROGRAM????()INTERFACE? ? OR API OR APIS
S11	27958	(NONVOLATILE OR NON()VOLATILE OR PERSISTENT OR PERMANENT) (-3N)(STOR???? OR MEMOR???)
S12	46	S1(S)S2:S3(S) (S11 OR S5) (S)S6(S)S7:S8
S13	24743	(S2:S3 OR S5 OR S11 OR MEMOR???) (5N) (FILE? ? OR OBJECT? ? OR DOCUMENT? ? OR CONTENT)
S14	46	S1(S)S2:S3(S) (S11 OR S5) (S)S13(S)S7:S8
S15	102798	(S2:S5 OR MEMOR???) (5N) (DATA OR INFORMATION OR RECORD? ?)
S16	213349	(ACCESS? OR RETRIEV? OR OBTAIN? OR FIND??? OR SEARCH??? OR TRACK???) (5N) (DATA OR INFORMATION OR RECORD? ?)
S17	172484	(TABLE? ? OR DIRECTOR??? OR REPOSITOR??? OR DATABASE? ? OR DATA()BASE? ? OR LIST???) (5N) (DATA OR INFORMATION OR RECORD? ?)
S18	458	S1(S)S2:S3(S) (S11 OR S5) (S)S15(S)S16:S17
S19	428	S18 NOT S14
S20	148	S19 AND IC=G06F
S21	41	S20/AB,CM
S22	8	S19/AB NOT S21
S23	143	S1(S)S2(S)S4
S24	127	S23 NOT (S14 OR S21:S22)
S25	14	S24/AB,CM
S26	45	S24 AND IC=G06F
S27	55	S25:S26
S28	1829	S1(S)S2(S)S11
S29	177	S28(S)S15(S)S16:S17
S30	137	S29 NOT (S14 OR S21:S22 OR S27)
S31	27	S30 AND IC=G06F
S32	18	S30/AB,CM
S33	44	S31:S32

14/5,K/1 (Item 1 from file: 348)
DIALOG(R) File 348:EUROPEAN PATENTS
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01370283

IC CARD

CHIPKARTE

CARTE A CIRCUIT INTEGRE

PATENT ASSIGNEE:

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LEGAL REPRESENTATIVE:

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PATENT (CC, No, Kind, Date): EP 1278154 A1 030122 (Basic)
WO 2001084490 011108

APPLICATION (CC, No, Date): EP 2000921094 000428; WO 2000JP2823 000428
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI;
LU; MC; NL; PT; SE

EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI

INTERNATIONAL PATENT CLASS: G06K-019/07

CITED PATENTS (WO A): JP 2061680 U ; JP 63009586 A ; JP 9259045 A ; JP
10334205 A ; JP 5057635 B2

ABSTRACT EP 1278154 A1

A multifunction IC card (MFC) has compatibility with a multimedia card, an SD card, etc. in that connector terminals (#1 through #13) are disposed on a card substrate (1) in two rows in a zigzag fashion, and realizes multifunction facilities in that a memory card unit (3) and an SIM (Subscriber Identity Module) card unit (4) are respectively exclusively connected and mounted to predetermined terminals of the connector terminals (#1 through #13). The memory card unit (3) and the SIM card unit (4) are respectively separately provided with areas for storing secrete codes for security. Thus, one IC card is capable of implementing multifunction facilities different in security level. Owing to the adoption of a plural-column layout corresponding to a form typified by the zigzag fashion in an array of the connector terminals, a relatively simple structure can be adopted in a card slot, wherein the amounts of protrusion of slot terminals in a card slot are alternately changed in association with a zigzag section, and the slot terminals are disposed in a row in parallel as a whole.

ABSTRACT WORD COUNT: 180

NOTE:

Figure number on first page: 1

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application: 020102 A1 International application. (Art. 158(1))
Application: 020102 A1 International application entering European
phase
Application: 030122 A1 Published application with search report

Examination: 030122 A1 Date of request for examination: 20021119
LANGUAGE (Publication,Procedural,Application): English; English; Japanese
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200304	1088
SPEC A	(English)	200304	8223
Total word count - document A			9311
Total word count - document B			0
Total word count - documents A + B			9311

...SPECIFICATION memory address is associated with the authorization code and set to the authorization code management table 36 of the security circuit 34. Thereafter, the multifunction IC card MFC is detached from the cellular phone 20 and attached to a reproduction terminal device or the like this time. In response to an access request sent from the terminal device, the interface controller 30 of the multifunction IC card MFC causes the security circuit 34 to determine, using the authorization code management table 36, whether a memory address of a file intended for access...

...into the flash memory 8 at its manufacturing stage is established. The authorization code management table 36 may be made up of an electrically rewritable non - volatile memory . The authorization code management table 36 may be placed in the interface controller 30 or the flash memory 8.

Once a secrete identification code is...

14/5,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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01310861

IC CARD AND METHOD FOR MANAGING VOLATILE MEMORY OF THE IC CARD
CHIPKARTE UND VERFAHREN ZUR VERWALTUNG EINES FLUCHTIGEN SPEICHERS AUF
DERSELBEN

CARTE A CIRCUIT INTEGRE ET PROCEDE DE GESTION DE LA MEMOIRE VOLATILE DE LA
CARTE A CIRCUIT INTEGRE

PATENT ASSIGNEE:

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Tokyo 105, (JP), (Applicant designated States: all)

INVENTOR:

KAWAURA, Atsuyoshi, 2016-2-408, Shimmachi 9-chome, Ome-shi, Tokyo
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LEGAL REPRESENTATIVE:

Kramer, Reinhold, Dipl.-Ing. et al (7031), Blumbach, Kramer & Partner
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PATENT (CC, No, Kind, Date): EP 1239411 A1 020911 (Basic)
WO 2001041058 010607

APPLICATION (CC, No, Date): EP 99974227 991130; WO 99JP6698 991130

DESIGNATED STATES: DE; FR; GB

EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI

INTERNATIONAL PATENT CLASS: G06K-019/073

ABSTRACT EP 1239411 A1

This invention has as its object to allow an IC card (2) to generate a volatile object , and to access the volatile object using a reference address on a nonvolatile memory (23).

These volatile objects are dynamically generated, and real objects are allocated in the order from volatile objects with shorter terms, so

as to allow garbage collection and reuse of a volatile memory (22), the term of which has expired.

ABSTRACT WORD COUNT: 72

NOTE:

Figure number on first page: 2

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application: 010801 A1 International application. (Art. 158(1))

Application: 010801 A1 International application entering European phase

Application: 020911 A1 Published application with search report

Examination: 020911 A1 Date of request for examination: 20020607

LANGUAGE (Publication,Procedural,Application): English; English; Japanese

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200237	522
SPEC A	(English)	200237	3457
Total word count - document A			3979
Total word count - document B			0
Total word count - documents A + B			3979

...ABSTRACT A1

This invention has as its object to allow an IC card (2) to generate a volatile object, and to access the volatile object using a reference address on a nonvolatile memory (23).

These volatile objects are dynamically generated, and real objects are allocated in the order from volatile objects with shorter terms, so as to allow garbage collection and reuse...

...SPECIFICATION storage address of the volatile storage unit corresponding to volatile data associated with this nonvolatile data in correspondence with each other.

Disclosure of Invention

An IC card of the present invention allows an application to generate a volatile object, and can access a volatile object in a volatile memory using a reference address in a nonvolatile memory.

Also, in a management method of a volatile memory in an IC card of the present invention, since volatile objects are always allocated at addresses...a nonvolatile object as a default, and becomes a volatile object by making library call using the reference to that object as an argument.

The IC card 2 has an object management unit 71 for managing volatile objects in the volatile memory 22 and nonvolatile objects in the data area 33 of the nonvolatile memory 23 using the nonvolatile object management table 34 and volatile object management table 44, as shown in FIG. 8.

Upon receiving reference address a called from an application, the object management unit 71 searches the nonvolatile object management...

14/5,K/3 (Item 3 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

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01046598

Intergrated circuit for embeddding in smart cards, and method of issuing smart cards

Integrierte Schaltung fur Einbettung in Chipkarten, und Verfahren zur

Herstellung von Chipkarten
Circuit integre pour encastrer dans des cartes a puce, et methode de fabrication de cartes a puce

PATENT ASSIGNEE:

Ok Electric Industry Co., Ltd., (225692), 7-12, Toranomom 1-chome
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INVENTOR:

Shona, Yoshihiro c/o Ok Electric Ind. C., Ltd, 7-12, Toranomom 1-chome,
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LEGAL REPRESENTATIVE:

Kirschner, Klaus Dieter et al (6509), Schneiders & Behrendt Rechtsanwälte
- Patentanwalte Sollner Strasse 38, 81479 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 926624 A2 990630 (Basic)
EP 926624 A3 000906

APPLICATION (CC, No, Date): EP 98118154 980924;

PRIORITY (CC, No, Date): JP 97358977 971226

DESIGNATED STATES: DE; FR; GB

EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI

INTERNATIONAL PATENT CLASS: G06K-019/073

ABSTRACT EP 926624 A2

An integrated circuit embedded in a smart card has a rewritable non-volatile memory in which an instruction file is stored. A control logic circuit in the integrated circuit converts random data into authentication data by executing instructions read from the instruction file, preferably by controlling a simplified data processing circuit having a shift register, an exclusive-OR logic circuit, and specialized bit operation circuits. A card issuer issuing smart cards including this integrated circuit writes different instruction files in different smart cards, thereby enhancing the security of the smart cards.

ABSTRACT WORD COUNT: 90

NOTE:

Figure number on first page: 1

LEGAL STATUS (Type, Pub Date, Kind, Text):

Search Report: 000906 A3 Separate publication of the search report
Application: 990630 A2 Published application (Alwith Search Report ;A2without Search Report)
Examination: 010502 A2 Date of request for examination: 20010306
Change: 991006 A2 Legal representative(s) changed 19990819

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9926	1042
SPEC A	(English)	9926	6210
Total word count - document A			7252
Total word count - document B			0
Total word count - documents A + B			7252

...SPECIFICATION object of the invention is to provide a method of using the invented integrated circuit that enhances the security of the smart cards.

The invented **integrated circuit** has an interface circuit for external input and output of commands and data, an electrically rewritable **non - volatile memory storing** at least one instruction **file** having a **list** of instructions, and an authentication data generator having logic circuits for executing the instructions, thereby converting random data into authentication data. The **integrated circuit** may also have a random data generator for generating the random data. The rewritable **non - volatile memory** preferably **stores** key

data as well as the instruction file.

In a preferred configuration, the authentication data generator has registers for storing the key data and random...

...CLAIMS further comprising the step of writing separate instruction files in said rewritable non-volatile memories (15) for use in authenticating said smart cards.

5. The integrated circuit (1) of claim 1, wherein said electrically rewritable non - volatile memory (15) stores a plurality of instruction files with different lists of instructions for generating said authentication data.
6. The integrated circuit (1) of claim 5, wherein said authentication data generator (17) selects one of said...

14/5,K/4 (Item 4 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

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00814713

Data exchange systems comprising portable data processing units

Datenaustauschsysteme mit tragbaren Datenverarbeitungseinheiten

Systemes d'echange de donnees comprenant des unites de traitement de donnees portatives

PATENT ASSIGNEE:

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, (Proprietor designated states: all)

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LEGAL REPRESENTATIVE:

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PATENT (CC, No, Kind, Date): EP 757336 A1 970205 (Basic)
EP 757336 B1 001122

APPLICATION (CC, No, Date): EP 95202143 950804;

PRIORITY (CC, No, Date): EP 95202143 950804

DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FR; GB; GR; IE; IT; LI; LU; NL; PT; SE

INTERNATIONAL PATENT CLASS: G07F-007/10; G06K-019/07

CITED PATENTS (EP B): EP 190733 A; EP 466969 A; EP 666550 A; WO 87/07062 A; WO 94/10657 A; DE 4126213 A

ABSTRACT EP 757336 A1

Data exchange system comprising at least one portable data processing unit (5) comprising data communication means (14), processing means (15) and memory means (16), the latter comprising an executive program (17) and one or more application descriptions (18(1) ... 18(n)), each application description comprising at least one interaction context (19(1) ...) comprising commands, data elements, data references, procedures, access conditions, and external references; the structure of the data elements and the data references as well as other references is chosen in such a way that a very efficient use of the restricted memory space of e.g. smart cards is obtained.

ABSTRACT WORD COUNT: 102

NOTE:

Figure number on first page: 3

LEGAL STATUS (Type, Pub Date, Kind, Text):

Grant: 001122 B1 Granted patent

Application: 970205 A1 Published application (A1with Search Report
;A2without Search Report)

Oppn None: 011114 B1 No opposition filed: 20010823
Examination: 971001 A1 Date of filing of request for examination:
970731
Change: 990721 A1 Title of invention (German) (change)
Examination: 990818 A1 Date of dispatch of the first examination
report: 19990624

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200047	2978
CLAIMS B	(German)	200047	2578
CLAIMS B	(French)	200047	3461
SPEC B	(English)	200047	11296
Total word count - document A			0
Total word count - document B			20313
Total word count - documents A + B			20313

14/5,K/8 (Item 8 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00589861

IC card with hierarchical file structure
IC-Karte mit hierarchischer Dateienstruktur
Carte IC avec structure de fichier hierarchique
PATENT ASSIGNEE:

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INVENTOR:

Takagi, Nobuya, 11-5, Suehiro-cho, Neyagawa-shi, Osaka-fu 572, (JP)
Mutoh, Yoshihiro, 4-18, Takada-cho, Ibaraki-shi, Osaka-fu 567, (JP)
Ueda, Masaaki, 5-2-308, Myokenzaka, Katano-shi Osaka-fu 576, (JP)
Murai, Nobunari, 1-4-40-519, Nonakaminami, Yodogawa-ku, Osaka-shi,
Osaka-fu 532, (JP)
Nakatomi, Takeshi, 1-13-2, Moroguchi, Tsurumi-ku, Osaka-shi, Osaka-fu 538
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LEGAL REPRESENTATIVE:

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(DE)

PATENT (CC, No, Kind, Date): EP 583006 A2 940216 (Basic)
EP 583006 A3 940518
EP 583006 B1 980909

APPLICATION (CC, No, Date): EP 93112836 930811;
PRIORITY (CC, No, Date): JP 92215817 920813; JP 92279884 921019
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06K-019/07; G06K-019/073;
CITED PATENTS (EP A): EP 479655 A; WO 9213322 A; FR 2635891 A

ABSTRACT EP 583006 A2

An integrated circuit card includes a processing controller, a non - volatile memory having plural files in a hierarchical structure, with each file having an access conditions controller relating to the level number of said hierarchical structure, and a RAM having plural key information fields corresponding to the level numbers. Each access condition controller has an access key box designation table which indicates which keys should be verified and a vertical matching condition settings table which indicates which level keys should be collected for verification. (see image in original document)

ABSTRACT WORD COUNT: 90

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application: 940216 A2 Published application (A1with Search Report
;A2without Search Report)
Examination: 940216 A2 Date of filing of request for examination:
930811
Change: 940511 A2 Obligatory supplementary classification
(change)
Search Report: 940518 A3 Separate publication of the European or
International search report
Examination: 970528 A2 Date of despatch of first examination report:
970410
Grant: 980909 B1 Granted patent
Oppn: 990804 B1 Opposition 01/990609 GEMPLUS SCA; Parc
d'activites de Gemenos BP 100; 13881 GEMENOS
Cedex; (FR)

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9837	369
CLAIMS B	(German)	9837	329
CLAIMS B	(French)	9837	413
SPEC B	(English)	9837	4430
Total word count - document A			0
Total word count - document B			5541
Total word count - documents A + B			5541

...ABSTRACT A2

An integrated circuit card includes a processing controller, a non - volatile memory having plural files in a hierarchical structure, with each file having an access conditions controller relating to the level number of said hierarchical structure, and a RAM having plural key information fields corresponding to the level numbers. Each access condition controller has an access key box designation table which indicates which keys...

14/5,K/10 (Item 10 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

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00210133

IC card.

IC-Karte.

Carte a puce.

PATENT ASSIGNEE:

Toppan Printing Co., Ltd., (442920), 5-1, 1-chome, Taito, Taito-ku Tokyo, (JP), (applicant designated states: CH;DE;FR;GB;LI)

INVENTOR:

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Takahashi, Masashi, 2-5-10-206, Takiyama, Higashikurume-shi Tokyo, (JP)

LEGAL REPRESENTATIVE:

Tiedtke, Harro, Dipl.-Ing. et al (11949), Patentanwaltsburo

Tiedtke-Buhling-Kinne & Partner Bavariaring 4, D-80336 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 220718 A2 870506 (Basic)

EP 220718 A3 911204

EP 220718 B1 950308

APPLICATION (CC, No, Date): EP 86114972 861028;

PRIORITY (CC, No, Date): JP 85242429 851029

DESIGNATED STATES: CH; DE; FR; GB; LI

INTERNATIONAL PATENT CLASS: G06F-019/00; G06K-019/06;

CITED REFERENCES (EP A):

PATENT ABSTRACTS OF JAPAN vol. 8, no. 215 (P-305)(1652) October 2, 1984
& JP-A-59 98 395 (DAINIPPON INATSU K.K.) June 6, 1984
IBM TECHNICAL DISCLOSURE BULLETIN. vol. 13, no. 7, December 1970, NEW
YORK US pages 1956 - 1960; D.R. HOLLOMAN: 'Forward and backward
chaining of data areas ';

ABSTRACT EP 220718 A2

In an IC (integrated circuit) card (10), a CPU (central processing unit) (11) is connected to a data bus (18) and an address bus (19). A data memory (12) is connected to the data bus (18) and the address bus (19). The data memory (12) is a rewritable memory, such as EEPROM (electrically erasable programmable read only memory) or battery backed-up RAM (random access memory). The data memory (12) is segmented into a predetermined number of sectors each consisting of predetermined bytes. An external processing device (20), such as a terminal device is connected to the data bus (18) and the address bus (19), via a one-bit I/O line (21) and a port (17). The terminal device (20) supplies a processing instruction via the I/O line (21) to the third port (17). The CPU (11) receives the processing instruction via the data bus (18), analyzes the instruction, and reads out and executes the necessary program. The CPU (11) supplies the results of each processing to the terminal device (20), by way of the data bus (18), the port (17) and the I/O bus (21). The sectors of the data memory (12) are functionally classified into the data sector, the directory sector, the file control sector, and the memory control sector. These sectors, if necessary, are chained with one another. The data relating to the sector chain is registered in each sector. The directory sector stores the data concerning each application file . The memory control sector stores the data indicating how the entire memory area of the data memory is used. The file control sector stores the sector number of the directory file .

ABSTRACT WORD COUNT: 276

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application: 870506 A2 Published application (A1with Search Report
;A2without Search Report)
Search Report: 911204 A3 Separate publication of the European or
International search report
Change: 911204 A2 Obligatory supplementary classification
(change)
Change: 920115 A2 Representative (change)
Examination: 920513 A2 Date of filing of request for examination:
920311
Examination: 930707 A2 Date of despatch of first examination report:
930525
Grant: 950308 B1 Granted patent
Oppn None: 960228 B1 No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	1151
CLAIMS B	(English)	EPAB95	1112
CLAIMS B	(German)	EPAB95	967
CLAIMS B	(French)	EPAB95	1407
SPEC A	(English)	EPABF1	5732
SPEC B	(English)	EPAB95	5726
Total word count - document A			6883
Total word count - document B			9212
Total word count - documents A + B			16095

...ABSTRACT A2

In an IC (integrated circuit) card (10), a CPU (central processing unit) (11) is connected to a data bus (18) and an address bus (19). A data memory (12) is connected to the data bus (18) and the address bus (19). The data memory (12) is a rewritable memory, such as EEPROM (electrically erasable programmable read only memory) or battery backed-up RAM (random access memory). The data memory (12) is segmented into a predetermined number of sectors each consisting of predetermined bytes. An external processing device (20), such as a...

...18), the port (17) and the I/O bus (21). The sectors of the data memory (12) are functionally classified into the data sector, the **directory** sector, the **file** control sector, and the **memory** control sector. These sectors, if necessary, are chained with one another. The data relating to the sector chain is registered in each sector. The directory sector stores the data concerning each application **file** . The **memory** control sector stores the data indicating how the entire memory area of the data **memory** is used. The **file** control sector stores the sector number of the **directory** **file** .

14/5,K/11 (Item 11 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00208712

Portable electronic device.

Tragbares elektronisches Gerat.

Dispositif electronique portatif.

PATENT ASSIGNEE:

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Iijima, Yasuo c/o Patent Division, Kabushiki Kaisha Toshiba 1-1 Shibaura
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LEGAL REPRESENTATIVE:

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PATENT (CC, No, Kind, Date): EP 218176 A2 870415 (Basic)
EP 218176 A3 880914
EP 218176 B1 911113

APPLICATION (CC, No, Date): EP 86113432 860930;

PRIORITY (CC, No, Date): JP 85223112 851007; JP 86114151 860519; JP
86150432 860626

DESIGNATED STATES: DE; FR; GB

INTERNATIONAL PATENT CLASS: G07F-007/10; G06F-009/26;

CITED PATENTS (EP A): EP 57602 A; EP 89876 A; EP 152024 A

CITED REFERENCES (EP A):

PATENT ABSTRACTS OF JAPAN, vol. 9, no. 329 (P-416) 2052 , 24th December
1985; & JP-A-60 153 582 (KIYODOU INSATSU K.K.) 13-08-1985

IBM TECHNICAL DISCLOSURE BULLETIN, vol. 22, no. 5, October 1979, pages
2009-2010, New York, US; A.J. SUTTON et al.: "Processors sharing and
partitioning of main storage in the MP system";

ABSTRACT EP 218176 A2

According to a portable medium (IC card) of this invention, a memory
area is divided into a system program area (4a) and a user program area

(4b). A text transmitted between the IC card and a host system (10) connected thereto includes a command text and a response text. The command or response text includes a flag indicating that the text is written in the user program area or the system program area. The memory area (43) has a conversion table for a function code and the start address of a program corresponding to the function code. The conversion table is looked up using the given function code as a parameter, thereby obtaining the start address of the corresponding program. The memory area (43) has a correspondence table between a newly added function code and the start address of an added function program. The added function program is selectively executed.

ABSTRACT WORD COUNT: 154

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application: 870415 A2 Published application (A1with Search Report
;A2without Search Report)
Examination: 870415 A2 Date of filing of request for examination:
861027
Search Report: 880914 A3 Separate publication of the European or
International search report
Examination: 890628 A2 Date of despatch of first examination report:
890512
Grant: 911113 B1 Granted patent
Oppn None: 921111 B1 No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	704
CLAIMS B	(German)	EPBBF1	586
CLAIMS B	(French)	EPBBF1	872
SPEC B	(English)	EPBBF1	4511
Total word count - document A			0
Total word count - document B			6673
Total word count - documents A + B			6673

...SPECIFICATION clock signal terminal; 2d, a reset signal terminal; 2e through 2g, data input/output terminals; and 2h, a write power source voltage (+21 V) terminal.

IC card 1 comprises control CPU (Central Processing Unit) 3, data memory 4 comprising a PROM for storing a control program, an identification number (e.g., 4 digits), and data, and interface circuit 5, as shown in Fig. 2. The respective...

...CPU 3 consists of a start code, a text length, a command code, a reference, data (variable length), and a check code (a check sum code or a value obtained by exclusively ORing respective data), as shown in Fig. 4. For example, an addition mode command consists of a code indicating addition of a command (command code), a code from the next time (reference), i.e., a code corresponding to an object program added by this command code, and an object program (data).

A response text consists of a start code, a text length, a command code (copy), a status (processing result, e.g., "write operation is completed"), data (variable length), and a check code (a check sum code or a value obtained by exclusively ORing text data), as shown in Fig. 5. The command and response texts have different text formats in accordance with whether they are written in area 4a or 4b. For example, in the case of the command text, when the first bit (MSB or LSB) of the command code is "1", this represents that the text is written in area 4b, and when it is "0", this represents that the text is written in area 4a. Meanwhile, when the first bit of the status code for the

response text is "1", this represents that...

...written in area 4b, and when it is "0", this represents that the text is written in area 4a.

Figs. 6 and 7 show the **arrangement of IC card** manipulator 10 as a terminal according to the present invention. More specifically, reference numeral 11 denotes a CPU (Central Processing Unit); 12, a keyboard for...

14/5,K/12 (Item 12 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00159931

Financial transaction processing system using on IC card.

Finanzielle Transaktionen verarbeitendes System, das eine Chip-Karte verwendet.

Systeme pour le traitement de transactions financieres utilisant une carte.

PATENT ASSIGNEE:

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PATENT (CC, No, Kind, Date): EP 162221 A2 851127 (Basic)
EP 162221 A3 880302
EP 162221 B1 921111

APPLICATION (CC, No, Date): EP 85103117 850318;

PRIORITY (CC, No, Date): JP 8453949 840319; JP 8454966 840321

DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IT; LI; LU; NL; SE

INTERNATIONAL PATENT CLASS: G07F-007/10;

CITED PATENTS (EP A): DE 3222288 A; DE 3222288 A; GB 2011671 A; FR 2471003
A

CITED REFERENCES (EP A):

PATENT ABSTRACTS OF JAPAN, vol. 5, no. 64 (P-59) 736 , 30th April 1981; &
JP-A-56 14 369 (FUJITSU K.K.) 12-02-1981
NEUES AUS DER TECHNIK, nos. 4/5, 15th September 1980, page 2, W|rzburg,
DE; "Kreditkarte mit Tastenfeld (und Wiedergabeordnung)";

ABSTRACT EP 162221 A2

IC card and financial transaction processing system using the IC card.

An IC card comprises a read only memory (ROM) (3) in which fixed data necessary for financial transaction processing, such as bank number and a transaction processing program, are stored, a random access memory (RAM) (4) for storing data necessary for transaction processing, such as a kind of transactions and a transaction amount, a central processing unit (CPU) (2) for processing transaction data in accordance with the transaction processing program, a keyboard (6) for entering data into the RAM (4), and a display (5) for displaying the entered data. A customer enters necessary transaction processing data by operation of the keyboard (6), prior to transaction processing. Correspondingly, the CPU (2) makes the RAM (4) store the entered transaction data in a predetermined storage area in response to the kinds of transactions. When the IC card is inserted into the terminal at the time of transaction, an IC card reader

(15) of the terminal reads out the contents in the ROM (3) and RAM (4) and a controlling position (22) performs any of transactions such as payment, deposit and transfer in accordance with the transaction data in the RAM (4).

ABSTRACT WORD COUNT: 202

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application: 851127 A2 Published application (A1with Search Report
;A2without Search Report)
Change: 860212 A2 Representative (change)
Search Report: 880302 A3 Separate publication of the European or
International search report
Examination: 881012 A2 Date of filing of request for examination:
880809
Examination: 901107 A2 Date of despatch of first examination report:
900921
Grant: 921111 B1 Granted patent
Lapse: 930526 B1 Date of lapse of the European patent in a
Contracting State: CH 921111, LI 921111
Lapse: 930526 B1 Date of lapse of the European patent in a
Contracting State: CH 921111, LI 921111
Lapse: 930609 B1 Date of lapse of the European patent in a
Contracting State: CH 921111, LI 921111, NL
921111
Lapse: 930630 B1 Date of lapse of the European patent in a
Contracting State: CH 921111, LI 921111, NL
921111, SE 921111
Lapse: 930818 B1 Date of lapse of the European patent in a
Contracting State: BE 921111, CH 921111, LI
921111, NL 921111, SE 921111
Oppn None: 931103 B1 No opposition filed
Lapse: 940504 B1 Date of lapse of the European patent in a
Contracting State: AT 921111, BE 921111, CH
921111, LI 921111, NL 921111, SE 921111
Lapse: 991229 B1 Date of lapse of European Patent in a
contracting state (Country, date): AT
19921111, BE 19921111, CH 19921111, LI
19921111, LU 19930331, NL 19921111, SE
19921111,

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	312
CLAIMS B	(German)	EPBBF1	261
CLAIMS B	(French)	EPBBF1	373
SPEC B	(English)	EPBBF1	4708
Total word count - document A			0
Total word count - document B			5654
Total word count - documents A + B			5654

...SPECIFICATION number of the papers (step S59) and determines whether the counted amount coincides with the amount stored in advance in the RAM 4 of the IC card (step S60). If these amounts coincide with each other, the terminal transmits to the center CPU of the bank the transaction data read out from the ROM 3 and RAM 4 of the IC card (step S61). Thus, the center retrieves and renews the corresponding file in accordance with the transmitted data. As a result, a deposit transaction processing is terminated and then the content of transaction stored in the RAM 4 of the IC card is erased (step S62) and the IC card is returned to the customer

14/5,K/28 (Item 16 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00805796 **Image available**

**SYSTEM AND METHOD FOR FACILITATING MULTIPLE APPLICATIONS ON A SMART CARD
SYSTEME ET PROCEDE POUR FACILITER DES APPLICATIONS MULTIPLES SUR UNE CARTE
A PUCE**

Patent Applicant/Assignee:

CRYPTEC SYSTEMS INC, 475 Alberto Way, Los Gatos, CA 95032, US, US
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Inventor(s):

CARPER Todd, 19834 Merritt Drive, Cupertino, CA 95014, US,

Legal Representative:

WHITT Stephen R (agent), 1215 Tottenham Court, Reston, VA 20194, US,

Patent and Priority Information (Country, Number, Date):

Patent: WO 200139427 A1 20010531 (WO 0139427)

Application: WO 2000US32318 20001124 (PCT/WO US0032318)

Priority Application: US 99450028 19991129

Designated States: SG

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

Main International Patent Class: H04L-009/00

Publication Language: English

Filing Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 7327

English Abstract

A system and method for facilitating the operation of multiple applications (A and B) on a smart card (1) are disclosed. One application (A) may call another application (B), or leave a message for it. Applications are initialized, de-initialized (fully or partially), and re-initialized to accomplish inter-application operability.

French Abstract

La presente invention concerne un systeme et un procede permettant de faciliter l'execution d'applications multiples (A et B) sur une carte a puce (1). Une application (A) peut appeler une autre application (B), ou lui laisser un message. Les applications sont initialisees, deinitialisees (completement ou partiellement), et reinitialisees pour permettre l'exploitabilite entre applications.

Legal Status (Type, Date, Text)

Publication 20010531 A1 With international search report.

Examination 20011011 Request for preliminary examination prior to end of 19th month from priority date

Fulltext Availability:

Claims

Claim

... The method of claim 17, wherein the data record associated with the message data object comprises an address vector indicating a location in read/write memory at which the message data object is stored.

19

/5

2

3

FlGo 1
POWER - RAM 6
4 ROM 7
oo@
an pow.- READ/
1/0 CPU WRITE
RESET 0 1 8
CLK 9
3
FlGe2 2
SUBSTITUTE SHEET (RULE 26)
/5 R/W MEMORY 1 0
/J
GLOBAL VARIABLES
A@13
FILE DIRECTORY 20 APPLICATION A
A1
A2
A3

INIT
LIST
MESSAGE BOX 0000e1
SECURITY APPLICATION B
APPLICATION
RAM 1 1
B1 B2 I
- TJ A4
B3 B4 I
-- I L
MESSAGE Box
FlGo3
SUBSITWE SHEET (RULE 26)
/5
INIT APPLICATION A @@30
PARTIALLY...

...symbols)
U.S. : 710/102,100,101,129; 235/487,492;713/187,200
Documentation searched other than minimum documentation to the extent
that such documents are included in the fields searched Electronic
data base consulted during the international search (name of data base
and, where practicable, search terms used) EAST search: ' smart card ',
"application near2 initializ\$5'. 'operating system'
C. DOCUMENTS CONSIDERED TO BE RELEVANT
Category Citation of document, with indication, where appropriate, of the
relevant passages Relevant...

...6,003,134 A (KUO et al) 14 December 1999, abstract and figures I I and
12. I- 14i 15113,15/14,16
18
Further documents are listed in the continuation of Box C. See
patent family aimex. Special categories of cited documents: 'T' later
document published after the international filing date or...

14/5,K/29 (Item 17 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00798023 **Image available**

DATA STORAGE AND ACCESS SYSTEMS

SYSTEMES DE STOCKAGE ET D'ACCES A DES DONNEES

Patent Applicant/Assignee:

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TN22 4AN, GB, GB (Residence), GB (Nationality), (For all designated
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Patent Applicant/Inventor:

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RACZ Patrick Sandor, 19 Royal Square, St. Helier, Jersey JE1 4WA, GB, --
(Residence), GB (Nationality), (Designated only for: US)

Legal Representative:

LUCKHURST Anthony Henry William (agent), Marks & Clerk, 57-60 Lincolns
Inn Fields, London WC2A 3LS, GB,

Patent and Priority Information (Country, Number, Date):

Patent: WO 200131599 A1 20010503 (WO 0131599)

Application: WO 2000GB4110 20001025 (PCT/WO GB0004110)

Priority Application: GB 9925227 19991025

Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ

DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ

LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG

SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG

(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Main International Patent Class: G07F-017/16

International Patent Class: G07F-007/08

Publication Language: English

Filing Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 20471

English Abstract

Data storage and access systems are described for downloading and paying for data such as audio and video data, text, software, games and other types of data. A portable data carrier has an interface for sending and receiving data, non-volatile data memory for storing received content data and non-volatile payment validation memory for providing payment validation data to an external device. The carrier may also store a record of access made to the stored content, and content use rules for controlling access to the stored content. Preferred embodiments store further access control data and supplementary data such as hot links to web sites and/or advertising data. A complementary data access terminal, data supply computer system and data access device are also described. The combination of payment data and stored content data and, in preferred embodiments, use rule data, helps reduce the risk of unauthorised access to data such as compressed music and video data, especially over the internet.

French Abstract

L'invention porte sur des systemes de stockage et d'accès destinés au téléchargement et au paiement de données telles que des données audio et vidéo, textes, logiciels, jeux et autres types de données. Un support de données portable comporte une interface destinée à envoyer et recevoir des données, une mémoire restante pour le stockage de données reçues et une mémoire restante de validation de paiement envoyant des données de validation de paiement à un dispositif externe. Le support peut également stocker un enregistrement d'accès effectué sur le contenu enregistré, et

des regles d'utilisation de contenu permettant de commander l'accès au contenu enregistré. Selon des réalisations préférées, il est également possible d'accéder à des données de commande et à des données supplémentaire telles que des liens dynamiques sur des sites web et/ou des données publicitaires. Un terminal d'accès à des données complémentaires, un système informatique d'alimentation de données et un dispositif d'accès à des données sont également décrits. La combinaison de données de paiement et de données de contenus enregistrés et, selon des réalisations préférées, des données de règles d'utilisation, aident à minimiser les risques des accès non autorisés à des données telles que des données musicales et vidéo comprimées, notamment sur Internet.

Legal Status (Type, Date, Text)

Publication 20010503 A1 With international search report.

Examination 20010920 Request for preliminary examination prior to end of 19th month from priority date

Fulltext Availability:
Detailed Description

Detailed Description

... bus 222. Also coupled to the bus are an audio interface 228, a display 230 and user controls 232, for providing a user interface. A smart Flash card interface 224 is coupled to bus 222 for interfacing with a smart Flash card for retrieving and playing stored content data. Permanent program memory 236 stores program code for implementation by processor 238; this code may also be provided on a data carrier such as a ROM chip or disk 240...

14/5,K/31 (Item 19 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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00783323 **Image available**

SMART CARD TRANSACTION MANAGER

GESTIONNAIRE DE TRANSACTIONS DE CARTE A PUCE

Patent Applicant/Assignee:

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(Residence), US (Nationality)

Inventor(s):

CARPER Todd, 19834 Merritt Drive, Cupertino, CA 95014, US,

Legal Representative:

WHITT Stephen R (agent), 1215 Tottenham Court, Reston, VA 20194, US,

Patent and Priority Information (Country, Number, Date):

Patent: WO 200116874 A1 20010308 (WO 0116874)

Application: WO 2000US84 20000105 (PCT/WO US0000084)

Priority Application: US 99386287 19990831

Designated States: SG

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

Main International Patent Class: G06K-019/06

International Patent Class: G06K-005/00; G06K-007/00

Publication Language: English

Filing Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 7079

English Abstract

A transaction manager (61) is provided in a smart card operating system

which ensures data integrity during smart card transactions which change the value of a data object (41) stored on the smart card (10).

French Abstract

L'invention concerne un gestionnaire de transactions (61) compris dans un systeme de fonctionnement de carte a puce qui garantit l'integrite des donnees lors de transactions avec ladite carte. Ces transactions modifient la valeur d'un objet de donnees (41) stockee dans la carte a puce (10).

Legal Status (Type, Date, Text)

Publication 20010308 A1 With international search report.

Examination 20010802 Request for preliminary examination prior to end of 19th month from priority date

Fulltext Availability:

Claims

Claim

... only after successfully changing the data object, deleting the transaction data record and resetting the transaction data record indicator.

27 A method of activating a **smart card** to accomplish a transaction with a 1 5 terminal, the **smart card** comprising an **non - volatile memory** containing a **file directory** storing one or more data records and containing a transaction record indicator, the method comprising:

upon receiving power in the **smart card** , interrogating the transaction record

indicator; and

upon determining in response to the interrogation of the transaction record indicator that a transaction record is stored in **memory** , interrogating the **file directory** to locate the transaction record.

28 The method of claim 27, wherein each data record stored in the file directory comprises a type field, the...

14/5,K/32 (Item 20 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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00783221 **Image available**

SMART CARD MEMORY MANAGEMENT SYSTEM AND METHOD

SYSTEME ET PROCEDE DE GESTION DE MEMOIRE DE CARTE A PUCE

Patent Applicant/Assignee:

CRYPTTEC SYSTEMS INC, 475 Alberto Way, Los Gatos, CA 95032, US, US

(Residence), US (Nationality)

Inventor(s):

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HEMMO David, 12, rue Caillaux, F-75013 Paris, FR,

Legal Representative:

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Patent and Priority Information (Country, Number, Date):

Patent: WO 200116759 A1 20010308 (WO 0116759)

Application: WO 2000US80 20000105 (PCT/WO US0000080)

Priority Application: US 99386286 19990831

Designated States: SG

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

Main International Patent Class: G06F-012/00

International Patent Class: G06K-019/07

Publication Language: English

Filing Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 8371

English Abstract

A system and method for memory management in a smart card (10) are disclosed. The memory manager, preferably part of a true operating system, is the single device by which memory in the smart card (10) is allocated and deallocated. Memory allocation for new data objects and memory deallocation as the result of data object deletion are made by reference to a memory management record (30), preferably a bitmap, which is stored in RAM (22) and formed upon smart card (10) initialization.

French Abstract

L'invention concerne un systeme et un procede destines a la gestion de memoire dans une carte a puce (10). Le gestionnaire de memoire, de preference element d'un vrai systeme de fonctionnement, est le seul dispositif par l'intermediaire duquel la memoire de la carte a puce (10) est attribuee et liberee. On realise l'attribution de memoire pour des nouveaux objets de donnees et sa liberation en consequence de la suppression d'objet de donnees en prenant en reference un enregistrement de gestion de memoire (30), de preference une table de bits, qui est stockee dans une memoire vive (22) et constituee suite a l'initialisation de la carte a puce (10).

Legal Status (Type, Date, Text)

Publication 20010308 A1 With international search report.

Examination 20010802 Request for preliminary examination prior to end of 19th month from priority date

Fulltext Availability:

Detailed Description

Detailed Description

... a new data record is formed is explained below with reference to the flowchart in Fig. 7. In this example, it is assumed that the **smart card** I 0 has been successfully activated. Accordingly, a **file directory** is stored in **EPROM**. a memory management record has been formed in **RAM**, and the **smart card** ready to receive a terminal command.

21/5,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00845190

INTERACTIVE ENTERTAINMENT APPARATUS
INTERAKTIVE UNTERHALTUNGSVORRICHTUNG
APPAREIL DE DIVERTISSEMENT INTERACTIF

PATENT ASSIGNEE:

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BA Eindhoven, (NL), (Proprietor designated states: all)

INVENTOR:

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FREITAG, Rosa, 21 Brook Road, Strawberry Vale, London N2 9RB, (GB)

LEGAL REPRESENTATIVE:

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PATENT (CC, No, Kind, Date): EP 789969 A1 970820 (Basic)

EP 789969 B1 030319

WO 97008891 970306

APPLICATION (CC, No, Date): EP 96926534 960826; WO 96IB847 960826

PRIORITY (CC, No, Date): GB 9517788 950831

DESIGNATED STATES: DE; ES; FR; GB; IT

INTERNATIONAL PATENT CLASS: H04N-005/765; A63F-013/10; G06F-017/30;
H04N-005/272

CITED PATENTS (EP B): EP 431723 A; WO 94/13105 A; WO 94/17886 A; WO
94/27677 A

CITED REFERENCES (EP B):

PATENT ABSTRACTS OF JAPAN, Vol. 18, No. 621, P-1832; & JP,A,06 236 138,
(GAKKEN CO LTD), 23 August 1994.;

NOTE:

No A-document published by EPO

LEGAL STATUS (Type, Pub Date, Kind, Text):

Change: 030312 A1 International Patent Classification changed:
20030118

Application: 970625 A1 International application (Art. 158(1))

Grant: 030319 B1 Granted patent

Application: 970820 A1 Published application (A1with Search Report
;A2without Search Report)

Change: 971029 A1 Inventor (change)

Examination: 971105 A1 Date of filing of request for examination:
970908

Examination: 991117 A1 Date of dispatch of the first examination
report: 19990930

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200312	868
CLAIMS B	(German)	200312	822
CLAIMS B	(French)	200312	966
SPEC B	(English)	200312	6350

Total word count - document A 0

Total word count - document B 9006

Total word count - documents A + B 9006

...CLAIMS other and prior to said further branch point (96).

2. Apparatus as claimed in Claim 1, further comprising a smart card

reader (60) operable to access data stored in a non - volatile memory of a smart card (58) and to write data thereto, wherein said interaction memory means comprises said memory of said smart card (58).

3. Apparatus as claimed in Claim 2, wherein image data from said image frame source (16,26) is in encrypted form and requires one...

21/5,K/2 (Item 2 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

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00312447

IC card and IC card information processing system using the IC card

Informationsverarbeitungssystem mit IC-Karte

Systeme informatique avec carte de CI

PATENT ASSIGNEE:

Hitachi Maxell Ltd., (227750), No 1-1-88, Ushitora Ibaraki-shi, Osaka-fu, (JP), (Proprietor designated states: all)

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Sugawara, Ken, 1468-5 Furumagi Ishigemachi, Yuki-gun Ibaraki-ken, (JP)

Yamauchi, Satoru, 1468-5 Furumagi Ishigemachi, Yuki-gun Ibaraki-ken, (JP)

Shinagawa, Tohru, 2-2-203 Togashira-1-chome, Toride-shi, (JP)

Miyamoto, Keiji, 6-9 Kubogaoka-3-chome Moriyamachi, Kitasoma-gun

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PATENT (CC, No, Kind, Date): EP 292237 A2 881123 (Basic)

EP 292237 A3 900425

EP 292237 B1 950208

EP 292237 B2 000301

APPLICATION (CC, No, Date): EP 88304457 880517;

PRIORITY (CC, No, Date): JP 87122288 870519; JP 87122289 870519

DESIGNATED STATES: DE; FR; GB

INTERNATIONAL PATENT CLASS: G06F-015/76

CITED PATENTS (EP A): EP 77404 A; EP 77404 A; WO 8000383 A; WO 8000383 A;

EP 167044 A

CITED PATENTS (EP B): EP 77404 A; EP 152024 A; EP 157303 A; EP 167044 A; EP

193635 A; EP 194893 A; EP 220718 A; WO 80/00383 A; US 3906460 A

CITED REFERENCES (EP A):

PATENT ABSTRACTS OF JAPAN, vol. 10, no. 225 (P-484), 6th August 1986; &

JP-A-61 60 131 (TOSHIBA)

IDEM;

CITED REFERENCES (EP B):

PATENT ABSTRACTS OF JAPAN, vol. 10, no. 225 (P-484), 6th August 1986 &

JP-A-61 60 131;

ABSTRACT EP 292237 A2

A non-volatile storage (3) and a volatile storage (4) having a shorter access time than that of the non-volatile storage are incorporated in an IC card (5), and the contents of the non-volatile storage is transferred to the volatile storage. In executing processings, an operation/processing unit (1) can access the volatile storage to perform processings at high speeds. Of multiple processing programs of a multi-functional IC card, only a selected program on the volatile storage can be executed.

ABSTRACT WORD COUNT: 82

LEGAL STATUS (Type, Pub Date, Kind, Text):

Amended: 20000301 B2 Amended patent

Application: 881123 A2 Published application (A1with Search Report
;A2without Search Report)
Amended: 20000301 B2 Date of patent maintained as amended:
20000301
Search Report: 900425 A3 Separate publication of the European or
International search report
Examination: 901010 A2 Date of filing of request for examination:
900818
Examination: 921216 A2 Date of despatch of first examination report:
921103
Grant: 950208 B1 Granted patent
Oppn: 960103 B1 Opposition 01/951102 GIESECKE & DEVRIENT GmbH;
Prinzregentenstrasse 159; D-81677 Munchen; (DE)
(Representative:) Klunker, Hans-Friedrich, Dr.;
Patentanwalte Klunker . Schmitt-Nilson . Hirsch
Winzererstrasse 106; D-80797 Munchen; (DE)

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200009	1350
CLAIMS B	(German)	200009	1143
CLAIMS B	(French)	200009	1519
SPEC B	(English)	200009	3678
Total word count - document A			0
Total word count - document B			7690
Total word count - documents A + B			7690

...CLAIMS program and data stored in the non-volatile storage for execution.

4. An IC card as claimed in claim 1 or claim 2, wherein the **storage means** includes non- **volatile first storage** means (3) for storing the processing programs and data, and second storage means (4) having a **shorter access time than that of the first storage** means, wherein the operation/processing unit (1) is operable to transfer the processing programs and/ **or data** of the first storage means to the second storage means, to access the second storage means to fetch the processing programs and/or data and...
- ...when the IC card is inserted in an external information processing unit (10) or the operation/processing unit receives a predetermined control signal.
7. An **IC card** as claimed in claim 5, wherein after completion of data exchange between the external unit and the operation/processing unit (1), the operation/processing unit...of that data within the first storage means.
11. An IC card as claimed in any of claims 3 to 10, wherein the first storage **means** (3) is an **EEPROM** and the second storage means (4) is an SRAM.
12. An IC card as claimed in any of claims 3 to 11, wherein the memory...

21/5,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00287247

Data processing system with pluggable option card.

Datenverarbeitungssystem mit einer steckbaren optionellen Karte.

Dispositif de traitement de donnees avec une carte optionnelle enfichable.

PATENT ASSIGNEE:

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Armonk, N.Y. 10504, (US), (applicant designated states:
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Langgood, John Kennedy, 271 N.W. 39th Place, Boca Raton Florida 33431,
(US)
Valli, Ronald Eugene, 104 McAllister Drive, Pittsburgh, PA 15235, (US)
LEGAL REPRESENTATIVE:
Burt, Roger James, Dr. (52152), IBM United Kingdom Limited Intellectual
Property Department Hursley Park, Winchester Hampshire SO21 2JN, (GB)
PATENT (CC, No, Kind, Date): EP 281999 A2 880914 (Basic)
EP 281999 A3 890823
EP 281999 B1 930602
APPLICATION (CC, No, Date): EP 88103609 880308;
PRIORITY (CC, No, Date): US 21391 870313
DESIGNATED STATES: AT; BE; CH; DE; ES; FR; GB; GR; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS: G06F-009/44; G06F-012/06;
CITED PATENTS (EP A): EP 136178 A; EP 136178 A; EP 136178 A; EP 171073 A;
EP 182044 A
CITED REFERENCES (EP A):
NEW ELECTRONICS, vol. 19, no. 14, 8th July 1986, pages 27-28, London, GB;
M. BUDZINSKI: "Geographic addressing with multibus II"
EDN MAGAZINE, vol. 26, no. 3, February 1981, page 88, Boston, US; N.D.
MACKINTOSH: "Interrogation tells mumP which boards are present";

ABSTRACT EP 281999 A2

A data processing system includes a central processing unit (CPU), a main memory unit, and input/output (I/O) sockets, each adapted to receive a selected one of a plurality of different and/or similar option cards. Each card contains (or is connected to) and controls a respective peripheral device, and each card is pre-wired with an ID value corresponding to its card type. Programmable option registers on each card store parameters such as address information, priority levels, and other system resource parameters. A setup routine, during initial power-on, retrieves and stores the appropriate parameters in the I/O cards and also in socket locations in main memory, one location being assigned to each input/output socket. Each socket location is adapted to hold the parameters associated with the card inserted in its respective socket and the card ID value. That portion of main memory containing the socket locations is adapted to maintain the parameter and ID information by means of battery power when system power fails or is disconnected, i.e., a non-volatile memory portion. Subsequent power-on routines are simplified by merely transferring parameters from the memory to the card registers if the status of all the sockets has not changed since the last power-down.

ABSTRACT WORD COUNT: 204

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application: 880914 A2 Published application (A1with Search Report
;A2without Search Report)
Examination: 890315 A2 Date of filing of request for examination:
890117
Change: 890816 A2 Obligatory supplementary classification
(change)
Search Report: 890823 A3 Separate publication of the European or
International search report
Change: 910220 A2 Representative (change)
Examination: 910403 A2 Date of despatch of first examination report:
910220
Change: 910814 A2 Representative (change)

Grant: 930602 B1 Granted patent
Change: 930922 B1 Representative (change)
Oppn None: 940525 B1 No opposition filed
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	627
CLAIMS B	(German)	EPBBF1	651
CLAIMS B	(French)	EPBBF1	680
SPEC B	(English)	EPBBF1	3515
Total word count - document A			0
Total word count - document B			5473
Total word count - documents A + B			5473

...CLAIMS to a like plurality of input/output option cards (5-0 to 5-7) each storing identifier data relating to the option provided thereby, characterised by a non - volatile memory (10) for storing , for each socket, identifier data relating to a card occupying such socket together with operational data for controlling execution of the associated option, means (14) for applying an enabling signal to said sockets at power on to obtain identifier data from each card occupying a socket, means (8) for comparing the identifier data so obtained with identifier data retained at power down in said non - volatile memory for cards occupying corresponding sockets to determine whether the retained operational data is valid for cards currently occupying the sockets and gating means (45) responsive...

21/5,K/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00076268

Microcomputer system.

Mikrocomputersystem.

Système de micro-ordinateur.

PATENT ASSIGNEE:

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PATENT (CC, No, Kind, Date): EP 63458 A2 821027 (Basic)
EP 63458 A3 850529
EP 63458 B1 890823

APPLICATION (CC, No, Date): EP 82301871 820408;

PRIORITY (CC, No, Date): US 253452 810413; US 253642 810413; US 253644
810413; US 276412 810622

DESIGNATED STATES: DE; FR; GB; NL

INTERNATIONAL PATENT CLASS: G06F-015/06; G06F-009/26; G06F-009/46;

CITED PATENTS (EP A): US 3990054 A; US 3980991 A

ABSTRACT EP 63458 A2

Microcomputer system.

A single-chip microcomputer device (10) contains a program memory or ROM (11) and a read/write data memory or RAM (12), along with an arithmetic/logic unit (ALU 14) and temporary address/data registers (PCL, PCH, T/MAH, MAL, IR) and busses (AL, AH, O, P, N, MD), all within a semiconductor integrated circuit constructed in a strip architecture. A number of 8-bit ports (A, B, C, D, 30) are used for data or address input/output, and for memory control, under control of registers (25) accessed by the memory data bus (MD). A counter (26) provides timer or event counter functions. The ports, memory control, and counter data and control, are all in the logical address space of both on-chip memory (11, 12) and off-chip memory. The microcomputer (10) is microcoded so each instruction word from ROM (11) generates an entry point address for a control ROM 17 to begin a sequence of microcode states using dispatch addressing in which the opcode is held in the instruction register (IR) to allow microjumps in the CROM addressing depending upon the memory address mode and the arithmetic/logic function. Various test and emulator functions are permitted, controlled by external pins.

ABSTRACT WORD COUNT: 197

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application: 821027 A2 Published application (A1with Search Report
;A2without Search Report)
Search Report: 850529 A3 Separate publication of the European or
International search report
Examination: 860212 A2 Date of filing of request for examination:
851129
Examination: 871125 A2 Date of despatch of first examination report:
871008
Grant: 890823 B1 Granted patent
Lapse: 900509 B1 Date of lapse of the European patent in a
Contracting State: NL 890823
Oppn None: 900808 B1 No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English

...ABSTRACT A2

Microcomputer system.

A single-chip microcomputer device (10) contains a program memory or ROM (11) and a read/write data memory or RAM (12), along with an arithmetic/logic unit (ALU 14) and temporary address/data registers (PCL, PCH, T/MAH, MAL, IR) and busses (AL, AH, O, P, N, MD), all within a semiconductor integrated circuit constructed in a strip architecture. A number of 8-bit ports (A, B, C, D, 30) are used for data or address input/output, and for memory control, under control of registers (25) accessed by the memory data bus (MD). A counter (26) provides timer or event counter functions. The ports, memory control, and counter data and control, are all in the logical address space of both on-chip memory (11, 12) and off-chip memory. The microcomputer (10) is microcoded so each instruction word from ROM (11) generates an entry point address for a control ROM 17 to begin a sequence of microcode states using dispatch addressing in which the opcode is held in the instruction register (IR) to allow microjumps...

21/5,K/11 (Item 7 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00867238 **Image available**

BIOMETRIC-BASED AUTHENTICATION IN A NONVOLATILE MEMORY DEVICE
AUTHENTIFICATION BIOMETRIQUE DANS UN DISPOSITIF A MEMOIRE NON VOLATILE

Patent Applicant/Assignee:

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US, US (Residence), US (Nationality), (For all designated states
except: US)

Patent Applicant/Inventor:

HASBUN Robert, Mortara Circle, Placerville, CA 95667, US, US (Residence),
US (Nationality), (Designated only for: US)

VOGT James, 4002 Tea Rose Court, El Dorado Hills, CA 95762, US, US
(Residence), US (Nationality), (Designated only for: US)

BRIZEK John, 3050 Marci Lane, Placerville, CA 95667, US, US (Residence),
US (Nationality), (Designated only for: US)

Legal Representative:

MALLIE Michael J (agent), Blakely Sokoloff Taylor & Zafman, LLP, 7th
Floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025, US,

Patent and Priority Information (Country, Number, Date):

Patent: WO 200201328 A2-A3 20020103 (WO 0201328)

Application: WO 2001US18692 20010607 (PCT/WO US0118692)

Priority Application: US 2000604682 20000627

Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU

CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP

KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD

SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG

(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Main International Patent Class: G07C-009/00

International Patent Class: G06F-001/00

Publication Language: English

Filing Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 6459

English Abstract

A biometric-based security circuit in which the user database, processor, and biometric map generation functions are all located on the same **integrated circuit** whose secure contents are inaccessible from external to the **integrated circuit**. Biometric data, such as a fingerprint, retina scan, or voiceprint, is taken from a user requesting access to restricted resources. The biometric data is transferred into **integrated circuit**, where it is converted to a biometric map and compared with a database of biometric maps **stored** in a **non - volatile memory** in the **integrated circuit**. The stored maps represents pre-authorized users, and a match triggers the security circuit to send a signal to a host processor authorizing the host processor to permit the requesting user access to the restricted resources. The **integrated circuit** essentially serves as a write-only **memory** for the secure **data**, because the secure data and security functions in the **integrated circuit** are not directly accessible through any pin or port, and therefore cannot be read or monitored through a dedicated security attack. A second **non - volatile memory**, accessible from external to the **integrated circuit**, can also be provided in the **integrated circuit** for holding non-secure **data**. This second **memory** has its own interface port, and is isolated from the security-related functions and memory so that secure and non-secure functions are physically isolated from each other and cannot be modified to overcome that isolation.

French Abstract

L'invention concerne un circuit de securite biometrique dans lequel la base de donnees utilisateur, le processeur et les fonctions de generation de cartes biometriques sont tous situes sur le meme circuit integre. Des donnees biometriques, telles qu'une empreinte digitale, retinienne ou vocale sont extraites d'un utilisateur demandant un acces a des ressources a diffusion restreinte. Ces donnees biometriques sont transferees au circuit integre, ou elles sont converties pour former une carte biometrique et comparees avec une base de donnees de cartes biometriques stockees dans une memoire non volatile dans ce circuit integre. Les cartes memorisees representent des utilisateurs pre-autorises et une concordance declenche ledit circuit de securite pour qu'il envoie un signal a un processeur hote autorisant celui-ci a permettre l'accès de l'utilisateur aux ressources a diffusion restreinte demandees. Ce circuit integre sert essentiellement de memoire a ecriture seule pour les donnees protegees, car les donnees protegees et les fonctions de securite comprises dans le circuit integre ne sont pas directement accessibles par une broche ou un port et, par consequent, ne peuvent etre lues ou surveillees par l'intermediaire d'une attaque de securite dediee. Ce circuit integre peut egalement etre equipe d'une seconde memoire non volatile pour le stockage de donnees non protegees. Cette seconde memoire, qui presente son propre port d'interface, est isolee des fonctions et de la memoire relatifs a la securite, de maniere que des fonctions protegees et non protegees sont physiquement isolees les unes des autres et ne peuvent etre modifiees de maniere a surmonter cette isolation.

Legal Status (Type, Date, Text)

Publication 20020103 A2 Without international search report and to be republished upon receipt of that report.

Search Rpt 20020606 Late publication of international search report

Republication 20020606 A3 With international search report.

Examination 20020906 Request for preliminary examination prior to end of 19th month from priority date

Fulltext Availability:

Claims

English Abstract

A biometric-based security circuit in which the user database, processor, and biometric map generation functions are all located on the same **integrated circuit** whose secure contents are inaccessible from external to the **integrated circuit**. Biometric data, such as a fingerprint, retina scan, or voiceprint, is taken from a user requesting access to restricted resources. The biometric data is transferred into **integrated circuit**, where it is converted to a biometric map and compared with a database of biometric maps **stored** in a **non - volatile memory** in the **integrated circuit**. The stored maps represents pre-authorized users, and a match triggers the security circuit to send a signal to a host processor authorizing the host processor to permit the requesting user access to the restricted resources. The **integrated circuit** essentially serves as a write-only **memory** for the secure **data**, because the secure data and security functions in the **integrated circuit** are not directly accessible through any pin or port, and therefore cannot be read or monitored through a dedicated security attack. A second **non - volatile memory**, accessible from external to the **integrated circuit**, can also be provided in the **integrated circuit** for holding non-secure **data**. This second **memory** has its own interface port, and is isolated from the security-related functions and

memory so that secure and non-secure functions are physically isolated...

Claim

... into the integrated circuit.

16 A method, comprising:

inputting a user's biometric data into an integrated circuit;

reading a database of previously stored biometric, **data** from a **non - volatile memory** in the **integrated circuit**, wherein contents of the **non - volatile memory** are

non-readable external to the **integrated circuit**;

comparing the user's biometric data with at least a portion of the database, using a

processor disposed on the **integrated circuit**;

sending a verification signal to an external device if comparing produces a match;

and

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sending a non-verification signal to the external device if...

...cause said at least one processor to perform:

inputting a user's biometric data into an integrated circuit;

reading a database of previously stored biometric **data** from a **non - volatile memory** in the **integrated circuit**, wherein contents of the **non - volatile memory** are

non-readable external to the **integrated circuit**;

comparing the user's biometric data with at least a portion of the database, using a

processor disposed on the **integrated circuit**;

24

sending a verification signal to an external device if comparing produces a match;

and

sending a non-verification signal to the external device if...

21/5,K/14 (Item 10 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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00818598 **Image available**

METHOD AND SYSTEM FOR OPTIMIZING ACCESS TO A COMMUNICATIONS NETWORK

PROCEDE ET SYSTEME D'OPTIMISATION DE L'ACCES A UN RESEAU DE TELECOMMUNICATIONS

Patent Applicant/Assignee:

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Patent and Priority Information (Country, Number, Date):

Patent: WO 200152084 A1 20010719 (WO 0152084)

Application: WO 2001US702 20010110 (PCT/WO US0100702)

Priority Application: US 2000175309 20000110

Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE
DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC
LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI
SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG

(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Main International Patent Class: G06F-015/173

Publication Language: English

Filing Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 8897

English Abstract

A method is disclosed for optimizing client access to a communication network. At least one disclosed embodiment of the method includes identifying (1010) a plurality of access points for a client to access a communication network from a specified location, and obtaining a plurality of metrics (1020), including a real-time performance metric, for each of the plurality of access points. The metrics can be evaluated (1030) by applying an evaluation algorithm and evaluation criteria to the metrics. At least one disclosed embodiment of the method also includes determining, using a processor, priority information (1040) for each of the plurality of access points based on the plurality of metrics for each of the plurality of access points, and providing the priority information regarding the access points to the client (1050).

French Abstract

La presente invention concerne un procede d'optimisation de l'acces client a un reseau de telecommunications. Au moins un mode de realisation de l'invention consiste a identifier (1010) une pluralite de points d'acces pour un client afin qu'il accede a un reseau de communication a partir d'un endroit specifie, et a obtenir une pluralite de mesures (1020), notamment une mesure du rendement en temps reel, pour chacun des points d'acces. On peut evaluer (1030) ces mesures en leur appliquant un algorithme d'evaluation et des criteres d'evaluation. Au moins un autre mode de realisation de l'invention consiste a determiner, au moyen d'un processeur, les informations de priorite (1040) pour chaque point d'acces sur la base de la pluralite de mesures pour chaque point d'acces, et a fournir ces informations de priorite aux clients (1050) selon les points d'acces.

Legal Status (Type, Date, Text)

Publication 20010719 A1 With international search report.

Publication 20010719 A1 Before the expiration of the time limit for
amending the claims and to be republished in the
event of the receipt of amendments.

Examination 20010920 Request for preliminary examination prior to end of

19th month from priority date

Fulltext Availability:
Claims

Claim

... 6020, the POP manager can collect real time data about the state of the networks from the servers. At activity 6030, the POP manager can obtain the POP cost rate information from the database. At activity 6040, the POP manager can obtain historical failure rates for each POP from the data base. At activity 6050, the POP manager can request the list of POPs and their DDO's for the next cluster on the list from the...

...or more POP manager information devices 7040 running the POP manager software 7045 can likewise be connected to network 7020, as can one or more database server information devices 7050, each serving one or more databases 7055. Any client 701 0 can provide to any server 703 0 a network string and/or...

...server 7030 can provide a log file to database 7055 and/or can receive from database 7055 a DDO. Database 7055 can 'de a POP list, failure information, cost information, and/or a cluster list to POP provi
manager 7045, which can compute the DDO's. POP manager 7045 can provide to database 7055 those computed DDO's.
Although shown...microprocessor, such the Pentium series microprocessor manufactured by the Intel Corporation of Santa Clara, California. In another embodiment, the processor can be an Application Specific Integrated Circuit (ASIC) that has been designed to implement in its hardware and/or firmware at least a part of a method in accordance with an embodiment...

...processor 8200 according to
one or more actions of any of methods 100 Memory 8300 can be any device capable of storing analog or digital information, such as a hard disk, Random Access
Memory (RAM), Read Only Memory (ROM), flash memory, a compact disk, a
magnetic tape, a floppy disk, etc., and any combination thereof
In one embodiment, instructions 8400 can be embodied in...

21/5,K/24 (Item 20 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00760627 **Image available**

A SEMICONDUCTOR MEMORY CARD, PLAYBACK APPARATUS, RECORDING APPARATUS,
PLAYBACK METHOD, RECORDING METHOD, AND COMPUTER-READABLE RECORDING
MEDIUM

CARTE MEMOIRE A SEMI-CONDUCTEURS, APPAREILS DE REPRODUCTION SONORE ET
D'ENREGISTREMENT, PROCEDES DE REPRODUCTION SONORE ET D'ENREGISTREMENT,
ET SUPPORT D'ENREGISTREMENT LISIBLE PAR ORDINATEUR

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Patent and Priority Information (Country, Number, Date):

Patent: WO 200074059 A1 20001207 (WO 0074059)

Application: WO 2000JP3297 20000524 (PCT/WO JP0003297)

Priority Application: JP 99149893 19990528; JP 99236724 19990824; JP
99372606 19991228

Designated States: BR CA CN ID RU SG

Main International Patent Class: G11C-007/00

International Patent Class: G06F-001/00; G06F-012/14

Publication Language: English

Filing Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 47581

English Abstract

An audio stream is divided into a plurality of audio object (AOB) files that are recorded having each been encrypted using a different encryption key. At least one piece of track management information (TKI) is provided corresponding to each track. Playlist information (PLI) assigns a playback position in a playback order to each track when a plurality of tracks are to be played back one after the other.

French Abstract

Selon la presente invention, une sequence audio est divisee en une pluralite de fichiers d'objets audio (AOB) qui sont enregistres apres cryptage au moyen d'une cle de cryptage differente. On realise au moins une information de gestion de piste (TKI) pour chaque piste. Une information de liste de diffusion (PLI) attribue a chaque piste un rang dans la liste de diffusion permettant de reproduire plusieurs pistes les unes apres les autres.

Legal Status (Type, Date, Text)

Publication 20001207 A1 With international search report.

Publication 20001207 A1 Before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments.

Fulltext Availability:

Claims

Claim

... the encryption key storing

file that stores a different encryption key for each AOB.

The recording apparatus may then process this **information** to **obtain** the TKMG and PLMG which it then **records** in the flash **memory** card.

(d) For ease of explanation, the recording apparatus and playback apparatus were described as being separate devices, though a portable playback apparatus can be...FIG. 68 can be achieved by executable programs that may be distributed and sold having been recorded on a recording medium. This recording medium may be an **IC card**, an optical disc, a floppy disk, or the like, with the programs recorded on the recording medium being used having first been installed into standard computer hardware. By performing

...to the flash memory card 31 to read the media ID (sc4) . The special region access control unit 324 obtains the media ID from the ROM 304 of the flash memory card 31 and passes it over to the playback apparatus (sc5) . The encryption/decryption circuit 327 then encrypts the media...to prove its own authenticity, the playback apparatus encrypts the challenge data (sc31) and sends the result to the authorization unit 321 in the flash memory card 31 as response data (sc32) The authorization unit 321 in 157 the flash memory card 31 encrypts the random number it sent as the challenge data (sc33) and compares...

...authentic.

In other words, the playback apparatus generates a random number (sc40) and sends this random number to the authorization unit 321 in the flash memory card 31 as challenge data (sc51) . In order to prove the authenticity of the flash memory card 31, the authorization unit 321 encrypts the challenge data (sc41) and sends the...

...as the challenge data (sc43) and compares this encrypted random number with the response data (sc44). 158

When the encrypted random number and there sponse data match, the f lash memory card 31 will be authenticated (OK) , and the playback apparatus will hereafter try to access the authentication region of the flash memory card 3 1. On the other hand, when the encrypted random number and the response data do not match, the flash memory card 31 will not be authenticated (NG) , and the playback apparatus will not try to access the authentication region of the flash memory card 31...

...As one alternative, each side may produce the secure key by taking a logical XOR of the encrypted challenge data produced by this side, response data received f rom the other side, and the secure media ID. The above embodiments have data that relates to the protection of copyrights stored in the authentication region...

21/5,K/31 (Item 27 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00457892 **Image available**

A SINGLE CHIP MICROCONTROLLER HAVING DOWN-LOADABLE MEMORY ORGANIZATION
SUPPORTING "SHADOW" PERSONALITY, OPTIMIZED FOR BI-DIRECTIONAL DATA
TRANSFERS OVER A COMMUNICATION CHANNEL
CONTROLEUR DE PERIPHERIQUES MICROPROGRAMME A PUCE UNIQUE DOTE D'UNE MEMOIRE
TELECHARGEABLE A PERSONNALITE "FANTOME", OPTIMISE POUR DES TRANSFERTS
DE DONNEES BIDIRECTIONNELS SUR UN CANAL DE COMMUNICATIONS

Patent Applicant/Assignee:

KLINGMAN Edwin E,

Inventor(s):

KLINGMAN Edwin E,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9848356 A1 19981029

Application: WO 98US8224 19980423 (PCT/WO US9808224)

Priority Application: US 97846118 19970424

Designated States: CA JP US AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL
PT SE

Main International Patent Class: G06F-013/00

International Patent Class: G06F-13:38

Publication Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 9072

English Abstract

A microcontroller down-loadable memory organization supporting "shadow" personality, optimized for connecting a computer system (66) to an ISDN network (64) to facilitate transmitting and receiving of data, the microcontroller (69) including a processor (136) and a memory structure having ROM memory space (156) for storing program code therein and further including a dual port RAM (134) for connection between the computer (66) and the processor (136), the dual port RAM (134) having RAM memory space (164) for storing program code therein and shared RAM (166) for storing data capable of being simultaneously accessible by the processor (136) and the computer (66), wherein the program ROM (156) and the program RAM (164) are selectively used by the computer (66) to store program code by the computer (66) using a ROM/RAM* select signal, and wherein the starting address in the shared RAM (166) wherein data is stored is selectably offset from the starting address of the code RAM (164) and the code ROM (156).

French Abstract

Ce controleur de peripheriques microprogramme a puce unique dote d'une memoire telechargeable a personnalite "fantome" est optimise aux fins d'un raccordement du systeme informatique (66) a un reseau numerique a integration de services (RNIS) (64) et ce, pour faciliter l'emission et la reception de donnees. Le controleur (69) de l'invention comprend un processeur (136) et une memoire a structure comportant un espace de memoire ROM (156) destine au stockage d'un code programme ainsi qu'un point de connexion double RAM (134) aux fins d'une connexion entre l'ordinateur (66) et le processeur (136), ce point de connexion double RAM (134) etant dote d'une espace de memoire RAM (164) destine au stockage d'un code programme et d'une memoire RAM partagee (166) destinee au stockage de donnees auxquelles peuvent simultanement acceder le processeur (136) et l'ordinateur (66). Les programmes RAM (164) et ROM (156) sont utilises de maniere selective par l'ordinateur (66) pour le stockage du code programme avec utilisation d'un signal de selection ROM/RAM*. L'adresse debut dans la memoire RAM partagee (166) ou sont stockees les donnees est decallee selectivement de l'adresse debut du code RAM (164) et du code ROM (156).

Fulltext Availability:

Claims

Claim

... from a group consisting of said dual port RAM and said program ROM depending upon the state of said ROM/RAM* signal.

10 A microcontroller **integrated circuit** as recited in claim 1 wherein said local processor further includes an internal **data RAM** for storing **data**, said internal **data RAM** accessible only by said local processor. 11 A microcontroller **integrated circuit** as recited in

claim I ftu-ther including an external **data RAM** coupled externally to the microcontroller **integrated circuit** through local processor signals generated by the local processor for storing **data** in said external **RAM** when the maximum addressable location of said dual port **RAM** is exceeded.

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SUBSTITUTE SHEET (RULE 26)

. A microcontroller for facilitating transfer of digital information from a host processor through a communication channel, comprising:
a local processor:

20/1

SUBSTITUTE SHEET (RULE 26)

a program **ROM** having storage locations addressable by said local processor, said

program **ROM** for storing program code;

a dual port **RAM** having storage locations addressable by the host processor and said local processor and having a predetermined storage area for storing data, said **data** storage area being

I , simultaneously **accessible** by the local processor and the host processor, whereby the host processor and said local processor can simultaneously **access** said **data** storage area and the host processor can further access said program storage area and said data storage when said local processor is in reset, and when said local processor is not in reset, said local processor can **access** said **data** storage space and said program storage space. I '). A microcontroller as recited in claim 12 wherein said **ROM** and **RAM** are addressed by the host through host address signals, host data signals, host bus control signal, and host interrupt signals.

14 A microcontroller as recited...

21/5,K/36 (Item 32 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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00298087 **Image available**

SECURE COMPUTER MEMORY CARD

CARTE MEMOIRE DE SECURITE POUR ORDINATEUR

Patent Applicant/Assignee:

TELEQUIP CORPORATION,

Inventor(s):

JONES Michael F,

ZACHAI Arthur,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9516238 A1 19950615

Application: WO 94US13898 19941205 (PCT/WO US9413898)

Priority Application: US 93161854 19931206

Designated States: AM AT AU BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GE HU

JP KE KG KP KR KZ LK LR LT LU LV MD MG MN MW NL NO NZ PL PT RO RU SD SE

SI SK TJ TT UA UZ VN KE MW SD SZ AT BE CH DE DK ES FR GB GR IE IT LU MC

NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG

Main International Patent Class: G06F-012/14

Publication Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 5925

English Abstract

A detachable PCMCIA memory card (100) incorporating a smartcard integrated circuit (250) for storing a password value and logic circuitry for preventing access to information stored on the memory card (100) unless the user of the host computer (110) to which the memory card (100) is connected can supply a password matching the stored password. The smartcard integrated circuit (250) may also be used to store public and private key values used to encrypt and decrypt data stored on the card (100) or elsewhere on the host computer (110) or exchanged with a remote computer (120).

French Abstract

La presente invention concerne une carte memoire PCMCIA (100) amovible comprenant un circuit integre (250) du type carte a memoire. Ce circuit integre permet de stocker la valeur d'un mot de passe et contient une logique de controle n'autorisant l'acces a l'information stockee par la carte memoire (100) que si l'utilisateur de l'ordinateur hote (110) auquel est connectee la carte memoire (100) peut fournir le mot de passe conforme au mot de passe stocke. Le circuit integre (250) de type carte a memoire peut egalement servir a stocker des valeurs de cles publiques et privees utilisables pour le chiffrement et le dechiffrement de donnees stockees sur la carte (100) ou ailleurs sur l'ordinateur hote, ou encore faisant l'objet d'echanges avec un ordinateur a distance (120).

Fulltext Availability:

Claims

Claim

... conductors in a personal computer connector socket, said interface conductors establishing data, address, control and power pathways between said card and
said personal computer,
a **non - volatile data storage memory** connected to said **data** and address pathways,
an **integrated circuit** comprising, in combination, a substorage **memory** unit for storing secret **data**, and means for processing a password supplied from said personal computer in accordance with said secret data to generate an authorization signal when said password has a predetermined correct value while otherwise preventing **access** to said secret **data** by means external to said **integrated circuit**, and
memory access control means for preventing said personal computer from **accessing data** stored in said **data storage memory** via said **data** and address pathways in the absence of said authorization signal.

2 A secure personal computer memory card as set forth in claim I wherein said...

21/5,K/41 (Item 37 from file: 349)

DIALOG(R) File 349:PCT FULLTEXT

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00140551 **Image available**

SMART CARD APPARATUS AND METHOD OF PROGRAMMING SAME

DISPOSITIF A CARTE INTELLIGENTE ET PROCEDE DE PROGRAMMATION

Patent Applicant/Assignee:

DATA CARD CORPORATION,
Inventor(s):
YOUNGER Thomas L,
Patent and Priority Information (Country, Number, Date):
Patent: WO 8705420 A1 19870911
Application: WO 87US509 19870306 (PCT/WO US8700509)
Priority Application: US 8695 19860310
Designated States: AT AU BB BE BG BJ BR CF CG CH CM DE DK FI FR GA GB HU IT
JP KP KR LK LU MC MG ML MR MW NL NO RO SD SE SN SU TD TG
Main International Patent Class: G06F-015/30
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 5196

English Abstract

A smart card (20) including a microcomputer (40). The microcomputer (40) being programmed with a smart card control program (50) and a data dictionary (52) defining the data to be stored in the microcomputer.

French Abstract

Carte intelligente (20) comprenant un micro-ordinateur (40). Dans le micro-ordinateur (40) est programme un programme de commande (50) de la carte intelligente ainsi qu'un dictionnaire de donnees (52) definissant les donnees pouvant etre memorisees dans le micro-ordinateur.

Fulltext Availability:
Claims

Claim

A method for making a **smart card** including a microcomputer; the method comprising the steps of:
a. programming the micro computer with a **smart card** control program;
b* defining data dictionary means for defining data stored in the microcomputer;
co programming the microcomputer with the data dictionary and personalized data.
2* A method in accordance with claim 1, wherein the step of programming the microcomputer with a **smart card** control program includes defining predetermined commands for accessing the **smart card** control program,
3e A method in accordance with claim 1, wherein the method of defining data dictionary means includes defining data dictionary means with a...

...the microcomputer with the data dictionary and personalized data includes the step of using a utility program at a terminal for interfacing with the **smart card** control program previously programmed in the microcomputer of the **smart card**,
5* A method in accordance with claim 1, wherein the step of programming the microcomputer with personalized data includes defining a data field ID, a...

...defining the data attribute includes defining the data as volatile non-volatile, or match, whereby if defined as match the personalized data stored in the **smart card** must match the data input thereby providing a security check.

A method in accordance with claim 1, wherein the step of defining the data dictionary means includes defining application specific data and personalized data.

8* A method for making a **smart card** including a microprocessor, the method comprising the steps of:

a. programming the microcomputer with a **smart card** control program;

be allocating **memory** for **data** dictionary means for defining data stored in the microcomputer;

co programming data values into the **data** dictionary area of **memory** ; and

de programming the microcomputer with personalized

data. 9* A method in accordance with claim 8, wherein volatile and non - volatile areas of **memory** are defined for storage of **data** .

He A method in accordance with claim 9, wherein the step of programming the microcomputer with a **smart card** control program includes defining commands for **retrieving** , storing, altering and protecting **data** .

110 A **smart card** having a microcomputer, comprising:

a. **smart card** control program means for controlling operation of the **smart card** , the **smart card** control program means defining predetermined commands for use in communicating with the **smart card** ;

be **data** dictionary means stored in **memory** for

defining **data** stored in the **smart card memory** , the **smart card memory** being divided into **volatile** and **non - volatile memory** ;

and

co the **smart card** control program including means for programming the **smart card** with application specific data, personalized data and transaction data.

?

27/5,K/8 (Item 8 from file: 348)
DIALOG(R) File 348:EUROPEAN PATENTS
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01196929

**SEMICONDUCTOR INTEGRATED CIRCUIT AND NONVOLATILE MEMORY ELEMENT
INTEGRIERTE HALBLEITERSCHALTUNG UND NICHTFLUCHTIGES SPEICHERELEMENT
CIRCUIT INTEGRE A SEMI-CONDUCTEUR ET ELEMENT DE MEMOIRE REMANENTE**

PATENT ASSIGNEE:

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LEGAL REPRESENTATIVE:

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PATENT (CC, No, Kind, Date): EP 1150302 A1 011031 (Basic)
WO 200046809 000810

APPLICATION (CC, No, Date): EP 2000900823 000119; WO 2000JP232 000119

PRIORITY (CC, No, Date): JP 9923631 990201

DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI;
LU; MC; NL; PT; SE

INTERNATIONAL PATENT CLASS: G11C-016/06

CITED PATENTS (WO A): US 5748532 A ; JP 6268180 A ; US 5764577 A ; EP
567707 A1; JP 10326837 A ; US 5862079 A

ABSTRACT EP 1150302 A1

An information retention capability based on a memory cell which comprises a pair of nonvolatile memory elements in a differential form is improved. A nonvolatile memory element (130) constituting a flash memory is so constructed that its tunnel oxide film (GO3) and floating gate electrode (FGT) are respectively formed by utilizing the gate oxide film (GT2) and gate electrode (GT2) of a transistor for a circuit which is formed on the same semiconductor substrate as that of the element (130). A memory cell is constructed in a 2-cells/1-bit scheme in which a pair of nonvolatile memory elements can be respectively connected to a pair of complementary data lines, and threshold voltage states different from each other are set for the nonvolatile memory elements so as to differentially read out data. A word line voltage in a readout mode is set to be substantially equal to a threshold voltage in a thermal equilibrium state (an initial threshold voltage), and also to be substantially equal to the average value of a low threshold voltage value and a high threshold voltage value. Thus, a data retention capability is enhanced to realize lowering in the rate of readout faults.

ABSTRACT WORD COUNT: 196

NOTE:

Figure number on first page: 1

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application: 001004 A1 International application. (Art. 158(1))
Application: 001004 A1 International application entering European
phase
Application: 011031 A1 Published application with search report
Examination: 011031 A1 Date of request for examination: 20010822

LANGUAGE (Publication,Procedural,Application): English; English; Japanese
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200144	2754
SPEC A	(English)	200144	20549
Total word count - document A			23303
Total word count - document B			0
Total word count - documents A + B			23303

...CLAIMS semiconductor integrated circuit as defined in Claim 4, wherein said floating gate is formed having an impurity of the first conductivity type.

6. A semiconductor integrated circuit as defined in Claim 5, further comprising a volatile storage circuit in which control information read out of said nonvolatile memory is held, and a volatile memory which includes a plurality of first volatile memory cells and second volatile memory cells and in which the first volatile memory cell is replaced with the second volatile memory cell in accordance with the control information transferred to said volatile storage circuit.
7. A semiconductor integrated circuit as defined in Claim 6, wherein said volatile memory is a cache memory, and that a central processing unit ...the allowable range of the gate film thicknesses based on the process deviations is approximately (+-)10% relative to a target film thickness.
26. A semiconductor integrated circuit as defined in Claim 20, further comprising a volatile storage circuit in which control information read out of said nonvolatile memory is held, and a volatile memory which includes a plurality of first volatile memory cells and second volatile memory cells and in which the first volatile memory cell is replaced with the second volatile memory cell in accordance with the control information transferred to said volatile storage circuit.
27. A semiconductor integrated circuit as defined in Claim 26, wherein said volatile memory is a cache memory, and that said cache memory is ...

27/5,K/14 (Item 14 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

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00626838

Microcomputer for IC card

Mikrorechner für IC-Karte

Microcalculatrice pour carte a circuits integres

PATENT ASSIGNEE:

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INVENTOR:

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1-17, Chuo 3-chome, Itami-shi, Hyogo 664, (JP)

LEGAL REPRESENTATIVE:

Leson, Thomas Johannes Alois, Dipl.-Ing. et al (78983), c/o TBK-Patent,
P.O. Box 20 19 18, 80019 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 610886 A2 940817 (Basic)
EP 610886 A3 941026
EP 610886 B1 011017

APPLICATION (CC, No, Date): EP 94101896 940208;

PRIORITY (CC, No, Date): JP 9321465 930209

DESIGNATED STATES: DE; FR; GB

INTERNATIONAL PATENT CLASS: G06F-001/00 ; G01R-031/317; G06F-011/00 ;
G06F-012/14 ; G06K-019/073
CITED PATENTS (EP B): EP 411255 A
CITED REFERENCES (EP B):
ELEKTRONIK, vol.37, no.22, 28 October 1988, MUNCHEN DE pages 204 - 208,
XP000051110 TIMM V. 'Mit einem EEPROM an Bord';

ABSTRACT EP 610886 A2

It is an object to obtain a microcomputer for an IC card arranged in such a manner that only a user mode can be performed after the microcomputer has been shipped to a user. A region on which shipment data representing a fact that the microcomputer has been shipped is written at the time of the shipment is formed in a test EEPROM region. A shipment confirmation routine for confirming whether or not the shipment data has been written is disposed to be performed before execution of a branch routine for branching to each program in accordance with an execution command supplied from outside. If the fact that the shipment data has been written on the test EEPROM region has been confirmed in a shipment confirmation routine, branching is limited to only the user mode. (see image in original document)

ABSTRACT WORD COUNT: 142

NOTE:

Figure number on first page: 1

LEGAL STATUS (Type, Pub Date, Kind, Text):

Change: 001102 A2 International Patent Classification changed:
20000913

Application: 940817 A2 Published application (A1with Search Report
;A2without Search Report)

Oppn None: 021009 B1 No opposition filed: 20020718

Grant: 011017 B1 Granted patent

Change: 020918 B1 Legal representative(s) changed 20020731

Search Report: 941026 A3 Separate publication of the European or
International search report

Change: 941026 A2 Obligatory supplementary classification
(change)

Examination: 950412 A2 Date of filing of request for examination:
950209

Examination: 991201 A2 Date of dispatch of the first examination
report: 19991019

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF2	779
CLAIMS B	(English)	200142	448
CLAIMS B	(German)	200142	394
CLAIMS B	(French)	200142	548
SPEC A	(English)	EPABF2	6883
SPEC B	(English)	200142	5571
Total word count - document A			7663
Total word count - document B			6961
Total word count - documents A + B			14624

INTERNATIONAL PATENT CLASS: G06F-001/00 ...

... G06F-011/00 ...

... G06F-012/14

...SPECIFICATION of a program of another person to copy or falsify the data.

Fig. 13 is a functional block diagram of a conventional microcomputer

for an IC card of the foregoing type. Referring to Fig. 13, reference numeral 1 represents a microcomputer for an IC card (hereinafter called a "microcomputer for a card"), 2 represents a CPU for processing data, 3 represents a mask ROM which is a **nonvolatile memory** in which a variety of programs are stored, 4 represents a RAM which is a **volatile memory** for temporarily **storing** data and 5 represents an input/output control circuit for controlling data input and output to and from an external device. Reference numeral 6 represents an EEPROM which is a write-enable **nonvolatile memory** for **storing** data of the results of the process or the like and 7 represents a bus for mutually connecting the foregoing elements. Reference numeral 8 represents...

...SPECIFICATION of a program of another person to copy or falsify the data. Fig. 13 is a functional block diagram of a conventional microcomputer for, an IC card of the foregoing type. Referring to Fig. 13, reference numeral 1 represents a microcomputer for an IC card (hereinafter called a "microcomputer for a card"), 2 represents a CPU for processing data, 3 represents a mask ROM which is a **nonvolatile memory** in which a variety of programs are stored, 4 represents a RAM which is a **volatile memory** for temporarily **storing** data and 5 represents an input/output control circuit for controlling data input and output to and from an external device. Reference numeral 6 represents an EEPROM which is a write-enable **nonvolatile memory** for **storing** data of the results of the process or the like and 7 represents a bus for mutually connecting the foregoing elements. Reference numeral 8 represents...

27/5,K/16 (Item 16 from file: 348)
DIALOG(R) File 348:EUROPEAN PATENTS
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00368723

Identification card.

Identifizierungskarte.

Carte d'identification.

PATENT ASSIGNEE:

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PATENT (CC, No, Kind, Date): EP 356237 A2 900228 (Basic)
EP 356237 A3 910130

APPLICATION (CC, No, Date): EP 89308600 890824;

PRIORITY (CC, No, Date): JP 88212065 880826

DESIGNATED STATES: DE; FR; GB

INTERNATIONAL PATENT CLASS: G07F-007/10; G06F-011/00

CITED PATENTS (EP A): EP 218176 A; EP 261335 A

ABSTRACT EP 356237 A2

An IC card includes a processor (1), a first memory (11) for storing therein a system program which runs on the processor (1) and which is associated with a basic operation of the IC card, a second memory (9) for storing therein an application program which runs on the processor (1) and which corresponds to a usage of the IC card, a third memory (8) for storing therein data processed by the processor (1), an input/output unit (2) for effecting input and output operations of programs and data, a

program stop section (6) for stopping the program being executed on the processor (1) at a specified address; and a data output section (4) for supplying the input/output unit (2) with either one of a content of a register in the processor (1) and a content of an area at an address of at least one of the first, second, and third memories (11, 9, 8) when the program running on the processor (1) is stopped.

ABSTRACT WORD COUNT: 169

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application: 900228 A2 Published application (A1with Search Report ;A2without Search Report)

*Assignee: 900816 A2 Applicant (transfer of rights) (change): Hitachi Maxell Ltd. (227750) No 1-1-88, Ushitora Ibaraki-shi Osaka-fu (JP) (applicant designated states: DE;FR;GB)

Search Report: 910130 A3 Separate publication of the European or International search report

Change: 910327 A2 Obligatory supplementary classification (change)

Examination: 910731 A2 Date of filing of request for examination: 910603

Examination: 930616 A2 Date of despatch of first examination report: 930429

Change: 940309 A2 Representative (change)

Refusal: 950322 A2 Date on which the European patent application was refused: 941105

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	766
SPEC A	(English)	EPABF1	4671
Total word count - document A			5437
Total word count - document B			0
Total word count - documents A + B			5437

...INTERNATIONAL PATENT CLASS: G06F-011/00

...SPECIFICATION execution to a terminal connected to the IC card, thereby evaluating the portion of the application program.

In order to achieve the objects above, the IC card according to the present invention includes a processor, a first nonvolatile memory section storing therein a basic processing program which runs on the processor to...

...an application program to be written depending on a purpose of the card after the card is manufactured, a third memory section comprising a rewritable nonvolatile or volatile memory for storing therein various processing data items, program initiate processing means for causing the processor to execute an application program (communicating data between the card and an external device) beginning from an execution start address set in the second nonvolatile memory section, program stop processing means for stopping an execution of the application program when a ...external device a content at least one selected from registers in the processor, other registers, an area indicated by a specified address of the second nonvolatile memory unit, and an area indicated by a specified address of the third memory unit such that at least one of the execution start address and...

...CLAIMS a stoppage in the application program and for keeping in place thereof a command code which can be executed by said processor (1).

5. An IC card comprising:
a processor (3);

a first **nonvolatile memory** section (11) for storing therein a basic processing program of said processor (3);
a rewritable second **nonvolatile memory** section (9) for storing therein an application program associated with the basic processing program;
a third memory section (8) comprising a rewritable **nonvolatile** or **volatile memory** for **storing** therein various kinds of processing data, thereby achieving data communications with an external device, said **IC card** further including:
program initiate processing means (5) for causing said processor (3) to execute the application program beginning from an execution start address set to said second **nonvolatile memory** section (9);
program stop means (6) operative during an execution of the application program for stopping the execution when a specified stop condition to stop...

...one of an internal register of said processor (3), another register, and at least one selected from areas indicated by addresses specified in said second **nonvolatile memory** section (9) and in said third memory section (8),
at least either one of the execution start address and the stop condition is set by...

27/5,K/33 (Item 15 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00796166 **Image available**

PARTITIONED MEMORY DEVICE HAVING CHARACTERISTICS OF DIFFERENT MEMORY TECHNOLOGIES
MEMOIRE PARTITIONNEE PRESENTANT DES CARACTERISTIQUES DE DIFFERENTES TECHNOLOGIES DE MEMOIRE

Patent Applicant/Assignee:

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Legal Representative:

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Patent and Priority Information (Country, Number, Date):

Patent: WO 200129672 A1 20010426 (WO 0129672)

Application: WO 2000US41243 20001018 (PCT/WO US0041243)

Priority Application: US 99420318 19991019

Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW (EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE (OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG (AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW (EA) AM AZ BY KG KZ MD RU TJ TM

Main International Patent Class: G06F-012/02

Publication Language: English

Filing Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 5009

English Abstract

A single-chip data processing circuit (100) has a memory management unit (200) and a homogeneous memory device (270). The memory management unit (i) partitions the homogeneous memory device to achieve heterogeneous memory characteristics for various regions of the memory device, and (ii) restricts access of installed applications executing in the microprocessor core to predetermined memory ranges. The memory management unit implements memory address checking using limit registers (325 and 345) and translates virtual addresses to an absolute memory address using offset registers (330 and 350). The memory management unit loads limit and offset registers with the appropriate values from an application table (300) to ensure that the executing application only accesses the designated memory locations.

French Abstract

L'invention concerne un circuit de traitement de données monopuce (100), qui comprend une unité de gestion mémoire (200) et une mémoire homogène (270). L'unité de gestion mémoire i) partitionne la mémoire homogène pour obtenir des caractéristiques de mémoire hétérogènes destinées à diverses zones de la mémoire; et ii) limite l'accès d'applications d'exécution installées dans le noyau du microprocesseur à des champs prédéterminés de la mémoire. L'unité de gestion mémoire effectue une vérification d'adresses mémoire au moyen de registres limites (325 et 345), et traduit des adresses virtuelles en une adresse mémoire absolue en utilisant des registres de désynchronisation (330 et 350). L'unité de gestion mémoire charge dans les registres limites et les registres de désynchronisation les valeurs appropriées tirées d'une table d'application (300) pour assurer que l'application d'exécution n'accède qu'aux emplacements de mémoire indiqués.

Legal Status (Type, Date, Text)

Publication 20010426 A1 With international search report.

Examination 20010913 Request for preliminary examination prior to end of 19th month from priority date

Correction 20020808 Corrected version of Pamphlet: pages 1/4-4/4, drawings, replaced by new pages 1/4-4/4; due to late transmittal by the receiving Office

Republication 20020808 A1 With international search report.

Main International Patent Class: **G06F-012/02**

Fulltext Availability:

Detailed Description

Detailed Description

... of certain information. In conventional smart cards, each memory type has been implemented using different technologies.

Byte erasable EEPROM, for example, is typically used to **store nonvolatile** data, that changes or configures the device in the field, while Masked-Rom and more recently one-time-programmable read-only memory (OTPROM) is typically used to store program code. The data and program code **stored** in such non- **volatile** **memory** will remain in memory, even when the power is removed from the **smart card**. **Volatile** memory is normally implemented as random access memory (RAM). The hardware technologies associated with each memory type provide desirable security benefits.

For example, the one-time...

...after each use.

There is an increasing trend, however, to utilize homogeneous memory devices, such as ferroelectric random access memory (FERAM), in the fabrication of smart cards. FERAM is a nonvolatile memory employing a ferroelectric material to store the information based on the polarization state of the ferroelectric material. Such homogeneous memory devices are desirable since they...

...the security benefits that were previously provided by the various hardware technologies themselves. Thus, a need exists for the ability to partition such otherwise homogeneous memory devices into volatile, non-volatile and program storage (ROM) regions with the appropriate corresponding memory characteristics.

United States Patent Number 5,890,199 to Downs discloses a system for selectively configuring a homogeneous...

27/5,K/44 (Item 26 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00461689 **Image available**

IC CARD WITH SHELL FEATURE

CARTE A CIRCUIT INTEGRE AVEC FONCTION INTERPRETEUR

Patent Applicant/Assignee:

MONDEX INTERNATIONAL LIMITED,

Inventor(s):

RICHARDS Timothy Philip,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9852153 A2 19981119

Application: WO 98GB1411 19980514 (PCT/WO GB9801411)

Priority Application: US 9746514 19970515; US 9746543 19970515; US 9875975 19980511

Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG

Main International Patent Class: G07F-007/10

International Patent Class: G06K-019/073

Publication Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 16158

English Abstract

There is provided an integrated circuit card having an associated operating mode. The integrated circuit card includes: a microprocessor; a memory coupled to the microprocessor; data stored in the memory representative of the operating mode; an operating system stored in the memory for processing selected information in a first IC card format; a shell application stored in the memory for processing the selected information in a second IC card format; and means for routing the selected information to either the operating system or the shell application responsive to the operating mode. The selected information may be a command, such as a file access command.

French Abstract

L'invention porte sur une carte a circuit integre possedant un mode de

fonctionnement associe et comprenant: un microprocesseur, une memoire couplee au microprocesseur; des donnees mises en memoire representant le mode de fonctionnement; un systeme d'exploitation mis en memoire pour traiter les informations selectionnees dans un premier format de carte a circuit integre; un interpreteur mis en memoire pour traiter les informations selectionnees dans un second format de carte a circuit integre; et un moyen d'acheminement des informations selectionnees soit vers le systeme d'exploitation, soit vers l'interpreteur reagissant au mode de fonctionnement. Les informations selectionnees peuvent etre une commande telle qu'une commande d'accès aux fichiers.

Fulltext Availability:
Claims

Claim
... stored on said IC card.

23 The method of claim 22, wherein a third data space for said third application is allocated which includes a **volatile memory** segment for referencing temporary data and non- **volatile memory** segment for referencing static data, wherein said third application's volatile segment includes a public and dynamic portion.

24 An apparatus for processing a plurality of applications stored in a memory of a single **integrated circuit** card comprising:
means for allocating a data space comprising at least a **nonvolatile memory** segment for referencing static data and a **volatile memory** segment for referencing temporary data; means for executing a first application; means for interrupting execution of said first application, means for saving data from at least a portion of said **volatile memory** segment; and means for executing a second application; means for retrieving said saved data; and means for completing said execution of said first application.
SUBSTITUTE...

27/5,K/45 (Item 27 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00439352 **Image available**

METHOD AND APPARATUS FOR COMBINING A VOLATILE AND A NONVOLATILE MEMORY ARRAY

PROCEDE ET APPAREIL PERMETTANT DE COMBINER DES MEMOIRES VOLATILES ET NON VOLATILES

Patent Applicant/Assignee:

INTEL CORPORATION,

Inventor(s):

PASHLEY Richard D,

WINSTON Mark D,

JUNGROTH Owen W,

KAPLAN David J,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9829816 A1 19980709

Application: WO 97US18425 19971014 (PCT/WO US9718425)

Priority Application: US 96777898 19961231

Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW GH KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM

GA GN ML MR NE SN TD TG
Main International Patent Class: G06F-013/00
International Patent Class: G11C-14:00; G11C-16:06
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 6608

English Abstract

An **integrated circuit** (IC) memory device (100) and method for interfacing **volatile** and non **volatile memory** arrays formed on a single semiconductor substrate. Data to be written from an external device such as a processor (104) is initially written to a **volatile** random access **memory** (RAM) write buffer array (101), and then written from the volatile RAM array (101) to a nonvolatile flash array (103) via an interface (102) to provide **nonvolatile data storage** at speeds typical of a RAM device. Data from first and second block addresses in the arrays may be merged in a flash merge buffer, and validity bits may be used to ensure data coherency. Data may be simultaneously written to or read from the volatile RAM array (101) during a time in which data is being read from or written to the nonvolatile flash array (103), which may be an EPROM or EEPROM.

French Abstract

L'invention porte sur une memoire de circuit integre (100) et un procede d'interfacage de reseaux de memoires volatiles et non volatiles places sur un meme substrat semi-conducteur. Les donnees a inscrire provenant d'un dispositif exterieur tel qu'un processeur (104) sont tout d'abord inscrites dans le reseau tampon (101) d'ecriture d'une RAM volatile puis transferees de la RAM (101) volatile sur un reseau de memoire flash (103) non volatile via une interface (102), ce qui permet le stockage non volatile a des vitesses propres aux RAM. Les donnees provenant d'adresses d'un premier et d'un deuxieme bloc des reseaux peuvent etre fusionnees dans un tampon flash et les bits de validite peuvent servir a assurer la coherence des donnees. Les donnees peuvent etre simultanement inscrites ou lues sur le reseau de memoire RAM (101) tout en etant inscrites ou lues sur le reseau flash non volatile (103) qui peut etre une EPROM ou une EEPROM.

Main International Patent Class: G06F-013/00
Fulltext Availability:
Detailed Description
Claims

English Abstract

An **integrated circuit** (IC) memory device (100) and method for interfacing **volatile** and non **volatile memory** arrays formed on a single semiconductor substrate. Data to be written from an external device such as a processor (104) is initially written to a **volatile** random access **memory** (RAM) write buffer array (101), and then written from the volatile RAM array (101) to a nonvolatile flash array (103) via an interface (102) to provide **nonvolatile data storage** at speeds typical of a RAM device. Data from first and second block addresses in the arrays may be merged in a flash merge buffer...

Detailed Description
... write capability.

Another desire of the invention is to provide a memory device for a

computer system that stores data in a nonvolatile manner.

An integrated circuit memory device comprising both volatile and nonvolatile memory arrays formed on a single semiconductor substrate is described. An interface is provided to couple the volatile memory array to the nonvolatile memory array. The interface is configured to write data to the volatile memory array, and to subsequently write that data from the volatile memory array to the nonvolatile memory array.

Other desires, features, and advantages of the present invention will be apparent from the accompanying drawings and the detailed description that follows.

BRIEF DESCRIPTION...

Claim

- 1 An integrated circuit memory device comprising:
a volatile memory array formed on a single semiconductor substrate;
a nonvolatile memory array formed on the single semiconductor substrate;
an interface that couples the volatile memory array to the nonvolatile memory array, the interface configured to write a first amount of data to the volatile memory array, and to subsequently write the first amount of data from the volatile memory array to the nonvolatile memory array.
- 2 . The memory device of claim 1 wherein the interface is formed on the single semiconductor substrate.
- 3 . The memory device of claim 1 wherein the interface is further configured to write the first amount of data from the volatile memory array to the nonvolatile memory array during at least a portion of a period of time in which a second amount of data is being written to the volatile memory array.
- 4 The memory device of claim 1 wherein the volatile memory array primarily comprises dynamic random access memory (DRAM), and the nonvolatile memory array...

27/5,K/46 (Item 28 from file: 349)
DIALOG(R) File 349:PCT FULLTEXT
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00428956 **Image available**
A CIRCUIT AND METHOD FOR ENSURING INTERCONNECT SECURITY WITHIN A MULTI-CHIP INTEGRATED CIRCUIT PACKAGE
CIRCUIT ET PROCEDE ASSURANT UNE SECURITE D'INTERCONNEXION AVEC UN BOITIER DE MICROCIRCUIT A PLUSIEURS PUCES
Patent Applicant/Assignee:
INTEL CORPORATION,
Inventor(s):
DAVIS Derek L,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9819420 A1 19980507
Application: WO 97US14442 19970815 (PCT/WO US9714442)
Priority Application: US 96735976 19961025
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ CZ DE DE

DK DK EE EE ES FI FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT
LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SK SL TJ TM TR
TT UA UG UZ VN YU ZW GH KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM
AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA
GN ML MR NE SN TD TG

Main International Patent Class: H04L-009/00

Publication Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 5259

English Abstract

Circuitry implemented within a multi-chip module (200) comprising a first integrated circuit chip (205) and a second integrated circuit chip (210) coupled together through an interconnect (215). Both the first and second integrated circuit chips include a cryptographic engine (245, 235) coupled to the interconnect and a non-volatile memory element (250, 230) used to contain key information (240). These cryptographic engines are solely used to encrypt outgoing information being output across the interconnect or to decrypt incoming information received from the interconnect. This prevents fraudulent physical attack of information transmitted across the interconnect.

French Abstract

L'invention concerne des circuits mis en oeuvre dans une module a plusieurs puces (200) comprenant une premiere (205) et une seconde puce (210), couplees au moyen d'une interconnexion (215). A la fois la premiere et la seconde puce comprennent un moteur de chiffrement (245, 235), couple a l'interconnexion, ainsi qu'un element de memoire non volatile (250, 230) utilise pour contenir les informations relatives aux cles (240). On utilise ces moteurs de chiffrement uniquement pour chiffrer des information sortantes; transmises par le biais de l'interconnexion, ou pour dechiffrer des informations entrantes recues a partir de cette interconnexion. Ce procede empeche toute attaque frauduleuse des informations transmises par le biais de l'interconnexion.

Fulltext Availability:

Claims

Claim

... a second cryptographic engine, said second cryptographic engine being coupled to the interconnect.

2 The multi-chip module according to claim 1, wherein said first **integrated circuit** chip further includes a non- **volatile memory** element, said **nonvolatile memory** element contains key information used by the first cryptographic engine for encryption of outgoing digital information before transmission over the interconnect and for decryption of incoming digital information received by the first cryptographic engine over the interconnect.

3 . The multi-chip module according to claim 1, wherein said second **integrated circuit** chip further includes a non- **volatile memory** element, said non **volatile memory** element contains key information used by the second cryptographic engine for encryption of outgoing digital information before transmission over the interconnect and for decryption of incoming digital information received by the second cryptographic engine over the interconnect.

4 . The multi-chip module according to claim 1, wherein said first

integrated circuit chip executes a stream cipher algorithm to encrypt the outgoing digital information and alternatively to decrypt the incoming digital information.

5 . The multi-chip module...a second cryptographic engine, said second cryptographic engine being coupled to the interconnect.

2 The multi-chip module according to claim 1, wherein said first integrated circuit chip further includes a non-volatile memory element, said nonvolatile memory element to contain key information to be used by the first cryptographic engine for encryption of outgoing digital information before transmission over the interconnect and...
...of incoming digital information received by the first cryptographic engine over the interconnect.

3 The multi-chip module according to claim 1, wherein said second integrated circuit chip further includes a non-volatile memory element, said nonvolatile memory element to contain key information to be used by the second cryptographic engine for encryption of outgoing digital information before transmission over the interconnect and...
decryption of incoming digital information received by the first cryptographic engine over the interconnect.

15 The computer system according to claim 13, wherein said second integrated circuit chip further includes a non-volatile memory element, said nonvolatile memory element to contain key information to be used by the second cryptographic engine for encryption of outgoing digital information before transmission over the interconnect and...

27/5,K/48 (Item 30 from file: 349)
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00409318 **Image available**
PORTABLE, SECURE TRANSACTION SYSTEM FOR PROGRAMMABLE, INTELLIGENT DEVICES
SYSTEME PORTABLE SUR DE GESTION TRANSACTIONNELLE DESTINE A DES UNITES
PROGRAMMABLES INTELLIGENTES

Patent Applicant/Assignee:

EUROPAY INTERNATIONAL N V,
HEYNS Guido,
JOHANNES Peter,

Inventor(s):

HEYNS Guido,
JOHANNES Peter,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9750063 A2 19971231

Application: WO 97EP3355 19970626 (PCT/WO EP9703355)

Priority Application: GB 9613450 19960627

Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES
FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN
MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG US UZ VN YU ZW
GH KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI
FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG

Main International Patent Class: G07F-007/10

International Patent Class: G06K-19:07

Publication Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 30297

English Abstract

The present invention provides a transaction management system for executing transactions between a first device (1) and a second device, said first and second devices being adapted for communication with each other and at least one of said first and second devices being an integrated circuit card, said system comprising: at least one input/output device (25); a portable virtual machine (20) for interpreting a computer program on said first device, said virtual machine comprising a virtual microprocessor and a driver for said at least one input/output device (25); and execution means responsive to said interpreted program for executing said program. The general linking technical concept behind the present invention is portability combined with security of data and run-time guarantees in a transaction system which are independent of the target implementation provided compile time checks are passed successfully. This concept is achieved by: using a virtual machine as an interpreter, including a driver for the I/O devices in the virtual machine so that application programs have a common interface with I/O devices and are therefore portable across widely differing environments, allocating and deallocating memory and including an indication of the amount of memory in the application program which means that the program will only run successfully or it will not run at all and security management functions are reduced to a minimum which improves operating speed, and providing a secure way of importing and exporting data in and out of application programs and databases.

French Abstract

La presente invention porte sur un systeme de gestion transactionnel permettant d'exécuter des transactions entre une premiere unite (1) et une deuxieme unite, lesdites premiere unite et deuxieme unite étant concues pour communiquer l'une avec l'autre. Au moins l'une desdites unites est une carte a circuit integre et un systeme comprenant: au minimum un dispositif d'entree/sortie (25), une machine virtuelle portable (20) pouvant interpreter un programme d'ordinateur sur ladite premiere unite, ladite machine virtuelle portable incluant un microprocesseur virtuel et un gestionnaire de peripheriques pour ledit ou lesdits dispositif(s) d'entree/sortie (25), et un moyen d'exécution répondant audit programme interprete pour exécuter ledit programme. Le concept technique general de liaison selon la presente invention est de combiner, dans un systeme de gestion transactionnelle, la portabilite, la securite des donnees et des garanties d'exécution, qui sont independantes de la mise en oeuvre visee pour autant que les verifications concernant la duree de compilation soient menees a bien. Ledit concept est realise au moyen d'une machine virtuelle utilisee comme interpreteur comprenant un gestionnaire de peripheries pour les dispositifs d'entree/sortie de la machine virtuelle (pour que les programmes d'application partagent la meme interface avec les dispositifs d'entree/sortie et deviennent ainsi portables dans des environnements tres differents). Le concept est aussi realise par attribution ou liberation de memoire et par indication de la quantite de memoire disponible pour le programme d'application (pour signifier que le programme tournera juste de maniere satisfaisante ou qu'il ne fonctionnera pas du tout ou que les fonctions de gestion de la securite sont reduites au minimum pour ameliorer la vitesse d'exécution). Le concept est en outre realise par la mise en place d'un moyen sur permettant d'importer ou d'exporter des donnees a partir de ou vers les programmes d'application ou bases de donnees.

Fulltext Availability:

Claims

Claim

... present invention. The present invention is however not limited

thereto. The ICC 5 includes at least an input/output (1/0) port IO and some **permanent storage**, e.g. a non- **volatile memory** which may be provided, for instance, by a EEPROM 15 connected to the 1/0 port I 0 via a bus 1 7 or ...battery-backed random access memory (RAM). The 1/0 port IO can be used for communication with the terminal I via card reader 7. An **integrated circuit** 1 5 card is a card into which one or more **integrated circuits** are inserted to perform at least memory functions. Optionally, the ICC 5 may be a self-contained portable intelligent card and include a read/writable working **memory** e.g. **volatile memory** provided by a RAM 14 and a central processor 12 as well as all necessary circuits so that card ICC 5 can operate as a...

...clock CLK to the sequencer 16. In accordance with the present invention the ICC 5 can be used as bank card, credit card, debit card, **electronic purse**, health card, SIM card or similar. The present invention provides an **integrated circuit** controlled transaction management system intended to execute between an ICC 5 and a terminal I connected or not connected to a central unit, a transaction...independent tokens and are resident on the terminal 1. The TRS main program loop will select and call TSS functions as needed by a particular **transaction**. * **Card** Selected Services (CS S) include functions supporting terminal transactions, such as payment service functions that are used as part of a TSS application. CSS are...loading the TRS module of the VM 20 (loading procedure is described later). Code for the VM 20 is stored in the terminal read only **nonvolatile memory** I 1. Before loading the TRS, the terminal **volatile memory** 19 of the terminal I is empty of all transaction related data, the terminal read/write non- **volatile memory** 18 contains the applications to be executed by the VM 20 in the form of modules 72 in a module repository, the non-volatile databases...

...If the VM 20 is also implemented upon an ICC 5, the same principles as described above apply with respect to the read only non- **volatile memory** 13, the **volatile memory** 14 and the read/write **nonvolatile memory** 15 of ICC 5. As VM 20 is a virtual machine it addresses all forms of terminal or ICC memory II, 18, 19; 13, 14...

...ICC 5 by a memory map or similar. In the following, reference will be made to volatile, read/write non-volatile and read only non- **volatile memory** as being part of the VM 20. It is to be understood that this refers to logically addressed memory space unless specific mention is made to actual addresses in an implementation of VM 20 on a terminal I or ICC 5. **Volatile memory** does not survive program loading or power-down and/or rebooting. Preferably, **volatile memory** does not survive power down for security reasons. **Nonvolatile memory** survives program loading or power-down and rebooting.

Virtual Machine description

A schematic representation of the VM 20 in accordance with the present invention is...data space 24 and which is treated by the VM 20 as random access memory (RAM) and would normally be implemented as part of the **volatile memory** 19, e.g. in RAM in an actual terminal I

27/5,K/50 (Item 32 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00346282 **Image available**
CHIP CARD WITH PROTECTED OPERATING SYSTEM
CARTE A PUCE AVEC SYSTEME D'EXPLOITATION PROTEGE
Patent Applicant/Assignee:

SIEMENS AKTIENGESELLSCHAFT,
WEINLANDER Markus,
Inventor(s):
WEINLANDER Markus,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9628795 A1 19960919
Application: WO 96DE399 19960306 (PCT/WO DE9600399)
Priority Application: DE 19508724 19950310
Designated States: CN FI NO SG UA US AT BE CH DE DK ES FI FR GB GR IE IT LU
MC NL PT SE
Main International Patent Class: G07F-007/10
Publication Language: German
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 1400
English Abstract

The invention concerns a **chip card** with at least one internal processor and a non- **volatile** programme **memory** for the operating system (BSC) of the processor. These are organized in such a way that the **chip card**, following its manufacture and its initial data-transfer connection to a read-write station, can only execute the at least one instruction statement which causes an operating-system-specific control table (KTB) to be reloaded into the **nonvolatile** programme **memory** of the processor, thus producing the assignment (adr 1...adr k... adr n) of user instruction statements (AWB x) to those parts of the operating system (BSC) which execute them. This has the advantage that the **chip card** is protected, in particular during the period between manufacture and delivery to the end-user, against unauthorized use, and its operating system against unauthorized access or alteration. The card preferably has means which cause the transmission of the control table (KTB) in encrypted form.

French Abstract

La presente invention concerne une carte a puce qui possede au moins un processeur interieur et une memoire de programmation non volatile, pour un systeme d'exploitation (BSC) du processeur. Ces elements sont organises de maniere que la carte a puce, apres sa fabrication et une premiere liaison informatique avec un poste d'ecriture et de lecture, ne puisse executer que l'unique instruction, qui est aussi le minimum, qui produit le chargement d'un tableau d'ordres (KTB) specifique au systeme d'exploitation dans la memoire de programmation non volatile du processeur. Cela realise la correspondance (adr1 ... adr k ... adr n) entre des instructions d'ordres pour l'utilisateur (AWBx) et les parties correspondantes du systeme d'exploitation (BSC) qui les executent. Cela presente l'avantage que la carte a puce est protegee contre l'utilisation non autorisee, en particulier pendant le laps de temps separant sa fabrication de sa remise a l'utilisateur final considere, et que son systeme d'exploitation est protege aussi contre la consultation et les modifications non autorisees. Un autre element avantageux est le fait qu'existent des moyens qui produisent le transfert du tableau d'ordres (KTB) sous une forme codee cryptographique.

English Abstract

The invention concerns a **chip card** with at least one internal processor and a non- **volatile** programme **memory** for the operating system (BSC) of the processor. These are organized in such a way that the **chip card**, following its manufacture and its initial data-transfer connection to a read-write station, can only execute the at least one instruction statement which causes an operating-system-specific control

table (KTB) to be reloaded into the **nonvolatile** programme **memory** of the processor, thus producing the assignment (adr 1...adr k... adr n) of user instruction statements (AWB x) to those parts of the operating system (BSC) which execute them. This has the advantage that the **chip card** is protected, in particular during the period between manufacture and delivery to the end-user, against unauthorized use, and its operating system against unauthorized access...

?

File 347:JAPIO Oct 1976-2002/Dec(Updated 030402)

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File 350:Derwent WPIX 1963-2003/UD,UM &UP=200324

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? ds

Set	Items	Description
S1	207325	(SMART OR CHIP OR STORED OR CRYPTO OR ACCESS OR SECURITY OR VALUE OR TRANSACTION? ? OR IC OR PAYMENT? ? OR PROGRAMMABLE)-(2W)CARD?? OR INTEGRATED()CIRCUIT? ? OR ELECTRONIC(1W)(PURSE?? OR WALLET?? OR CARD? ?)
S2	22744	(VOLATILE OR UNSTABLE OR NONPERSISTENT OR NON()PERSISTENT - OR TRANSIENT)(3N)(STOR???? OR MEMOR???)
S3	133668	RAM OR RANDOM()ACCESS()MEMORY OR DRAM OR SRAM OR SDRAM OR RDRAM OR SLDRAM OR SGRAM OR DRDRAM
S4	34099	(NONVOLATILE OR NON()VOLATILE OR PERSISTENT OR PERMANENT)(-3N)(STOR? OR MEMOR???)
S5	90285	ROM OR READ()ONLY()MEMORY OR PROM OR EPROM OR EEPROM
S6	69626	(S2:S4 OR MEMOR???) (5N)(FILE? ? OR OBJECT? ? OR PROGRAM? ? OR RECORD? ? OR SOFTWARE OR APPLICATION? ? OR DOCUMENT? ? OR CONTENT)
S7	240194	(ACCESS? OR STOR??? OR SAV??? OR RETRIEV? OR OBTAIN? OR GET???? OR FIND??? OR SEARCH??? OR TRACK??? OR HOUS??? OR MAINTAIN???) (5N)(FILE? ? OR OBJECT? ? OR PROGRAM? ? OR SOFTWARE OR APPLICATION? ? OR DOCUMENT? ? OR CONTENT)
S8	40208	(TABLE? ? OR DIRECTOR??? OR REPOSITOR??? OR DATABASE? ? OR DATA()BASE? ? OR LIST????) (5N)(FILE? ? OR OBJECT? ? OR PROGRAM? ? OR SOFTWARE OR APPLICATION? ? OR DOCUMENT? ? OR CONTENT)
S9	28956	(AUTHORIZ? OR AUTHORIS? OR CLEAR? OR CREDENTIAL? ? OR PERMISSION? ? OR PERMIT? OR ALLOW?) (5N)(FILE? ? OR OBJECT? ? OR PROGRAM? ? OR SOFTWARE OR APPLICATION? ? OR DOCUMENT? ? OR CONTENT)
S10	2171	APPLICATION()PROGRAM()INTERFACE? ? OR API OR APIS
S11	2638	S1 AND S2:S3 AND S4:S5
S12	603	S11 AND S6:S10
S13	0	S11 AND S6 AND S7 AND S8 AND S9 AND S10
S14	253	S11 AND S6 AND S7:S8
S15	150	S1/TI AND S14
S16	79	S15 AND S2 AND S4
S17	71	S15 NOT S16
S18	103	S14 NOT S15
S19	36	S18 AND (S2 OR S4)
S20	67	S18 NOT S19
S21	623	S1 AND VOLATILE AND ("NONVOLATILE" OR "NON-VOLATILE")
S22	590	S21 NOT S14
S23	2	S22 AND S6 AND S7:S8
S24	72407	(S2:S5 OR MEMOR???) (5N)(FILE? ? OR OBJECT? ? OR PROGRAM? ? OR SOFTWARE OR APPLICATION? ? OR DOCUMENT? ? OR CONTENT)
S25	4	S22 AND S24 AND S7:S8
S26	319	S11 AND S24 AND S7:S8
S27	67	S26 NOT S14
S28	63144	(ACCESS? OR RETRIEV? OR OBTAIN? OR FIND??? OR SEARCH??? OR TRACK???) (5N)(FILE? ? OR OBJECT? ? OR DOCUMENT? ? OR CONTENT)
S29	25	S11 AND S28
S30	3	S29 NOT (S14 OR S27)

16/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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06417865 **Image available**

IC CARD PROVIDED WITH MEMORY CONTENT SHIFT CONTROL PART, AND DATA
STORING METHOD FOR IC CARD

PUB. NO.: 2000-003424 [JP 2000003424 A]
PUBLISHED: January 07, 2000 (20000107)
INVENTOR(s): OBANA MANABU
OKUHARA SUSUMU
TAKEYABU HIDEKI
APPLICANT(s): HITACHI LTD
APPL. NO.: 11-047773 [JP 9947773]
FILED: February 25, 1999 (19990225)
PRIORITY: 10-107312 [JP 98107312], JP (Japan), April 17, 1998
(19980417)
INTL CLASS: G06K-019/07

ABSTRACT

PROBLEM TO BE SOLVED: To shorten the connection time between an IC card and an information processor by executing the processing of an IC card through the use of a high speed memory and reporting the end of the processing to the connected information processor when the processing is ended.

SOLUTION: A processing executing part 10 processes data which is received from the information processor in the IC card 100 through the use of a high speed volatile memory 151. Then, the processing end is reported to the information processor when data received by the processing executing part 110 is ended. When data with the necessity of preservation exists among data, a power supply control part 130 interrupts an external power source, it is changed-over into an internal power source and a memory contents shift control part 120 transfers data with the necessity of preservation in the non - volatile memory 152 with low memory updating speed from the volatile memory 151 and stores it. The IC card 100 is connected to the information processor by a communication line 180 and connected to an external power supply source by a power supply line 190.

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16/5/4 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO
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06184945 **Image available**

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUB. NO.: 11-126495 [JP 11126495 A]
PUBLISHED: May 11, 1999 (19990511)
INVENTOR(s): TANAKA TOSHIAKI
APPLICANT(s): CITIZEN WATCH CO LTD
APPL. NO.: 09-286747 [JP 97286747]
FILED: October 20, 1997 (19971020)
INTL CLASS: G11C-016/06; G11C-016/02

ABSTRACT

PROBLEM TO BE SOLVED: To obtain a program voltage generating circuit

for performing multi- value **storage** for **non - volatile memory** elements with a simple circuit without increasing chip area by adding a reference voltage and input data by using an adder circuit composed of an operational amplifier and plural MONOS type **memory** elements.

SOLUTION: The **program** voltage generator circuit block 13 is provided with four-first to fourth-MONOS type **non - volatile memory** elements 19, 21, 23, 25 composed of metal-silicon oxide-a nitride silicon film, a silicon oxide film, and constitutes an adder circuit by an OP amplifier and memory elements 19, 21, 23, 25. This adder circuit adds and outputs the reference voltage source 27 and the output voltage of the program level setting circuit 15 which sets a program level by input data 11. By this, the block 13 can generate a **program** voltage for multi-value **storage** to a **non - volatile memory** element 29 with a simple circuit.

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16/5/5 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO
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06131821 **Image available**
IC CARD

PUB. NO.: 11-073359 [JP 11073359 A]
PUBLISHED: March 16, 1999 (19990316)
INVENTOR(s): HAYASHI MASAHIRO
IRISAWA KAZUYOSHI
APPLICANT(s): DAINIPPON PRINTING CO LTD
APPL. NO.: 09-233941 [JP 97233941]
FILED: August 29, 1997 (19970829)
INTL CLASS: G06F-012/00; G06F-012/00; G06K-017/00

ABSTRACT

PROBLEM TO BE SOLVED: To improve transmission efficiency and security by executing the transfer of a file and reading of a history file in an **IC card** only by sending an instruction.

SOLUTION: The **IC card** having a CPU, a **RAM**, an electrically erasable and programmable **read - only memory** (**EEPROM**), and a **ROM** and including plural files in the **EEPROM** is provided with an access management means for managing an **access** to a **file** and a transfer/read means for circularly transferring/reading out data in a specified file to plural history files annexed to the specified file. A pointer indicating a latest written **file** is included in a **non - volatile memory**, a pointer indicating a latest read **file** is included in a **volatile memory** and the access management means executes access management based on the pointer information.

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16/5/6 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO
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05791802 **Image available**
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUB. NO.: 10-074902 [JP 10074902 A]
PUBLISHED: March 17, 1998 (19980317)
INVENTOR(s): KURODA KENICHI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 09-221405 [JP 97221405]
FILED: August 18, 1997 (19970818)
INTL CLASS: [6] H01L-027/10; G11C-016/04; H01L-021/8247; H01L-029/788;
H01L-029/792
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components); 45.2
(INFORMATION PROCESSING -- Memory Units)
JAPIO KEYWORD: R004 (PLASMA); R005 (PIEZOELECTRIC FERROELECTRIC SUBSTANCES);
R100 (ELECTRONIC MATERIALS -- Ion Implantation); R131
(INFORMATION PROCESSING -- Microcomputers & Microprocessors)

ABSTRACT

PROBLEM TO BE SOLVED: To improve degrees of freedom for a ROM by having a first non - volatile memory erasing an electrically written information by irradiation of ultraviolet ray and a second non - volatile memory electrically erasing information electrically written.

SOLUTION: A microcomputer provided with an central processing unit(CPU) 100 and a nonvolatile memory storing program data and dictionary data of the CPU 100 on one semiconductor chip 1 is constituted. The first non - volatile memory (EPROM) 105 electrically performs write of information and erases the written information by irradiation of an ultraviolet ray. The second non - volatile memory (EEPROM) 107 electrically performs write of informations and electrically erasing the written informations. In this way, a ROM with a large capacity and a capability for rewriting can be obtained and an electrically rewritable ROM on a system can be obtained.

16/5/7 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO
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05720426 **Image available**
IC CARD

PUB. NO.: 10-003526 [JP 10003526 A]
PUBLISHED: January 06, 1998 (19980106)
INVENTOR(s): WAKAMATSU MASAKI
HARIMA HIROTSUGU
APPLICANT(s): DAINIPPON PRINTING CO LTD [000289] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-153563 [JP 96153563]
FILED: June 14, 1996 (19960614)
INTL CLASS: [6] G06K-019/07; G06F-009/45; G06K-017/00
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 30.1
(MISCELLANEOUS GOODS -- Office Supplies); 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)

ABSTRACT

PROBLEM TO BE SOLVED: To provide an IC card in which an application program described in prescribed language can be introduced, regardless of a CPU which is being used.

SOLUTION: This IC card 10 is provided with a CPU 18, read only memory 12 which stores a general program which can be executed by the CPU 18, and reloadable non - volatile memory 16 which stores an

application program which can be executed by the CPU 18 according to need. In this case, the read only memory 12 has a language conversion program for converting a program described in a prescribed language into a program described in language which can be executed by the CPU 18, and the CPU 18 converts the application program applied from an outside part by using the language conversion program, and stores it in the non-volatile memory 12.

16/5/9 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO
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05720330 **Image available**
IC CARD AND PASSWORD PROCESSING PROGRAM EXECUTION METHOD

PUB. NO.: 10-003430 [JP 10003430 A]
PUBLISHED: January 06, 1998 (19980106)
INVENTOR(s): WAKAMATSU MASAKI
HARIMA HIROTSUGU
APPLICANT(s): DAINIPPON PRINTING CO LTD [000289] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-153597 [JP 96153597]
FILED: June 14, 1996 (19960614)
INTL CLASS: [6] G06F-012/14; G06K-017/00; G09C-001/00; H04L-009/10; H04L-009/14
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 44.3 (COMMUNICATION -- Telegraphy); 44.9 (COMMUNICATION -- Other); 45.3 (INFORMATION PROCESSING -- Input Output Units)

ABSTRACT

PROBLEM TO BE SOLVED: To provide an IC card which can speedily and inexpensively change a cipher processing program.
SOLUTION: The IC card is provided with a non-volatile memory 16 which can be rewritten, a read-only memory 12 storing a first cipher processing program ciphering information and CPU 18 ciphering information by using the first cipher processing program. The non-volatile memory has a cipher processing program area which can store a second cipher processing program different from the first cipher processing program. Then, CPU 18 ciphers information by using the second cipher processing program instead of the first cipher processing program when the second cipher processing program is stored in the cipher processing program area.

16/5/10 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO
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05720285 **Image available**
IC CARD AND APPLICATION PROGRAM INTRODUCING METHOD

PUB. NO.: 10-003385 [JP 10003385 A]
PUBLISHED: January 06, 1998 (19980106)
INVENTOR(s): WAKAMATSU MASAKI
MORIYAMA AKIKO
HARIMA HIROTSUGU
APPLICANT(s): DAINIPPON PRINTING CO LTD [000289] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-156626 [JP 96156626]

FILED: June 18, 1996 (19960618)
INTL CLASS: [6] G06F-009/06; G06F-009/445; G06K-019/07
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units);
45.3 (INFORMATION PROCESSING -- Input Output Units)

ABSTRACT

PROBLEM TO BE SOLVED: To provide an IC card, etc., with which an application program can be introduced without necessity to previously confirm the absolute address of a memory area for storing the program

SOLUTION: This IC card is provided with a CPU 18, a read only memory 12 for storing a general-purpose program to be executed by the CPU 18, and a reloadable non-volatile memory 16 for storing one or two more application programs to be executed by the CPU 18 as needed. In this case, this general-purpose program includes an address translation program for reloading a rearrangement enable CPU instruction code contained in this application program corresponding to the address of area where this application program is to be stored or is stored.

16/5/12 (Item 12 from file: 347)
DIALOG(R)File 347:JAPIO
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04602559 **Image available**
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUB. NO.: 06-274459 [JP 6274459 A]
PUBLISHED: September 30, 1994 (19940930)
INVENTOR(s): MATSUBARA KIYOSHI
SHIBATA KATSUNARI
YAMAOKA HIROMASA
WATABE MITSURU
KASAHARA TAKAYASU
MOROOKA YASUO
FUNABASHI SEIJU

APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)

APPL. NO.: 05-082739 [JP 9382739]

FILED: March 17, 1993 (19930317)

INTL CLASS: [5] G06F-015/16; G06F-011/20; G06F-013/36; G06F-013/36;
G06F-013/38; G11C-016/06; G11C-029/00; H01L-021/82;
H01L-027/04; G06F-009/44

JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 42.2
(ELECTRONICS -- Solid State Components); 45.1 (INFORMATION
PROCESSING -- Arithmetic Sequence Units); 45.2 (INFORMATION
PROCESSING -- Memory Units)

JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors,
MOS); R129 (ELECTRONIC MATERIALS -- Super High Density
Integrated Circuits, LSI & GS; R131 (INFORMATION
PROCESSING -- Microcomputers & Microprocessors

JOURNAL: Section: P, Section No. 1851, Vol. 18, No. 690, Pg. 49,
December 26, 1994 (19941226)

ABSTRACT

PURPOSE: To improve the versatility of a semiconductor integrated circuit device for realizing the combination of the plural kinds of processing.

CONSTITUTION: This device is equipped with a **non - volatile memory** in which the rewriting of information can be electrically attained as a microprogram memory, and the change of the **storage content** of the microprogram **memory** can be attained after the completion of LSI. Moreover, the device is equipped with a programmable switch array 105 for mutually connecting plural processors so as to be programmable, and the change of the connection relation among the plural processors can be attained after the completion of LSI. Thus, the versatility of LSI can be improved.

16/5/13 (Item 13 from file: 347)
DIALOG(R)File 347:JAPIO
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04355277 **Image available**
IC CARD

PUB. NO.: 05-346977 [JP 5346977 A]
PUBLISHED: December 27, 1993 (19931227)
INVENTOR(s): MUTO YOSHIHIRO
TAKAGI SHINYA
UEDA MASAACKI
MURAI NOBUNARI
NAKATOMI TAKESHI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company
or Corporation), JP (Japan)
APPL. NO.: 04-154625 [JP 92154625]
FILED: June 15, 1992 (19920615)
INTL CLASS: [5] G06K-019/07
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 30.1
(MISCELLANEOUS GOODS -- Office Supplies)
JOURNAL: Section: P, Section No. 1721, Vol. 18, No. 189, Pg. 97, March
31, 1994 (19940331)

ABSTRACT

PURPOSE: To provide the IC card which is improved in safety and throughput by hierarchically controlling a file and key data.

CONSTITUTION: Data from external equipment are received through an input/output means 5 and a command processing means 6 analyzes and processes the received data according to control information 8 as the collation result of a key stored in a **volatile memory** 3 and generates an answer corresponding to the received data. A file control means 7 is actuated by the command processing means 6 to perform centralized control over the data to be processed as a gathering of data, and **accesses** the file in a **nonvolatile rewritable memory** 9 or data in the file .

16/5/14 (Item 14 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2003 JPO & JAPIO. All rts. reserv.

04266423 **Image available**
TERMINAL SYSTEM WITH IC CARD

PUB. NO.: 05-258123 [JP 5258123 A]
PUBLISHED: October 08, 1993 (19931008)
INVENTOR(s): SASAGAWA YASUSHI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP

(Japan)
APPL. NO.: 04-053563 [JP 9253563]
FILED: March 12, 1992 (19920312)
INTL CLASS: [5] G06K-017/00; G06F-003/08; G06K-019/07
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units)
JOURNAL: Section: P, Section No. 1675, Vol. 18, No. 24, Pg. 131,
January 14, 1994 (19940114)

ABSTRACT

PURPOSE: To permit an incorporated **memory** to execute plural **application IC cards** without overflow in the same terminal mainbody with the **IC card**.

CONSTITUTION: The terminal mainbody with **IC card 10** is provided with one slot for **IC card 2**, and it incorporates a **non - volatile memory 3** and a **non - volatile memory 1** inside. Here, the regular **application IC card 20** and a **file management IC card 30** storing data which becomes necessary on the operation of an application program are provided as the cards which can be inserted into the slot for **IC card 2**.

16/5/16 (Item 16 from file: 347)
DIALOG(R)File 347:JAPIO
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03944039 **Image available**
SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE

PUB. NO.: 04-309139 [JP 4309139 A]
PUBLISHED: October 30, 1992 (19921030)
INVENTOR(s): SAWADA MASARU
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP
(Japan)
FUJITSU VLSI LTD [491219] (A Japanese Company or Corporation)
, JP (Japan)
APPL. NO.: 03-075242 [JP 9175242]
FILED: April 08, 1991 (19910408)
INTL CLASS: [5] G06F-011/28; G06F-011/22; G11C-016/04; H01L-021/82
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units);
42.2 (ELECTRONICS -- Solid State Components); 45.2
(INFORMATION PROCESSING -- Memory Units)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers &
Microprocessors)
JOURNAL: Section: P, Section No. 1503, Vol. 17, No. 129, Pg. 74, March
18, 1993 (19930318)

ABSTRACT

PURPOSE: To form a **non - volatile memory**, which can reload a **program**, and an **ICE circuit** on a chip and to change the contents of the **non - volatile memory** by the **ICE circuit**.

CONSTITUTION: A **non - volatile memory 1** stores the **program** so as to reload it, and a central processing unit(CPU) 2 is composed of an address generation circuit 2a equipped with a **program counter 2b** to perform **access** to the prescribed address of the **memory 1** and a **program execution part 2c** for the read-out **program**. A **RAM 3** stores data used for executing the **program**. An **ICE circuit 4** controls and supervises the operation of the CPU 2, a first stop control means 5 stops the operation of the program execution part 2c based on a write control signal inputted from an outside **ICE device** and a write control means 6 inputs

address data inputted from the outside ICE device to the address generation circuit 2a and writes program data in the prescribed address of the memory 1 accessed by the address generation circuit 2a.

16/5/18 (Item 18 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2003 JPO & JAPIO. All rts. reserv.

03075286 **Image available**
IC CARD AND ITS PROGRAM REWRITING SYSTEM

PUB. NO.: 02-050786 [JP 2050786 A]
PUBLISHED: February 20, 1990 (19900220)
INVENTOR(s): SHINAGAWA TORU
APPLICANT(s): HITACHI MAXELL LTD [000581] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-201218 [JP 88201218]
FILED: August 12, 1988 (19880812)
INTL CLASS: [5] G06K-019/07; B42D-015/10
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 30.1 (MISCELLANEOUS GOODS -- Office Supplies)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessors)
JOURNAL: Section: P, Section No. 1045, Vol. 14, No. 219, Pg. 159, May 09, 1990 (19900509)

ABSTRACT

PURPOSE: To shorten the program rewriting processing time of an IC card by storing a program data part to constitute a processing program in respective storing areas, providing a control information storing area to store control information indicating the substance of the storing area of the respective program data parts and making the control information of the area arbitrarily settable.

CONSTITUTION: A processing program executed by an operation processing part 3 and control information to divide a stored area into a data part and to control when the processing program is stored in a non - volatile memory 5 are stored in the rewritable non - volatile memory 5. Then, the operation processing part 3 refers to the control information corresponding to information to designate the one of the areas of the data part divided and controlled which is transmitted from an external device, obtains the storing area of the data part to be written and writes the data part to constitute the processing program in the storing area. Thus, it is satisfied with transmitting the data part necessary to be rewritten in the processing program from the external device simply, and it is not necessary to execute processing to rewrite the whole program at an IC card side.

16/5/19 (Item 19 from file: 347)
DIALOG(R)File 347:JAPIO
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03058191 **Image available**
IC CARD

PUB. NO.: 02-033691 [JP 2033691 A]
PUBLISHED: February 02, 1990 (19900202)
INVENTOR(s): KAWAKITA TATSUJIRO

APPLICANT(s): NIPPON TELEGR & TELEPH CORP <NTT> [000422] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-183652 [JP 88183652]
FILED: July 25, 1988 (19880725)
INTL CLASS: [5] G06K-019/07; B42D-015/10
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 30.1 (MISCELLANEOUS GOODS -- Office Supplies)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessors)
JOURNAL: Section: P, Section No. 1037, Vol. 14, No. 189, Pg. 11, April 17, 1990 (19900417)

ABSTRACT

PURPOSE: To prevent the unfair forging by providing an area having an address in the control of a memory control means at a **non - volatile memory** and an area having the special address outside the control and executing the writing through the control **program** of a **memory** control means.

CONSTITUTION: In a ROM 4, a program, etc., to write the program able to be executed by a microprocessor unit (MPU)6 from an external part into a **non - volatile memory** 3A are **stored** besides the program to control the **memory** space of the **non - volatile memory** 3A. An address control lower limit address 18 of the memory 3A able to be controlled by the **memory** control **program** of the ROM 4 and a control upper limit address 19 are recorded in a special address 17 of the ROM 4. The **memory** control **program** of the ROM 4 refers to the special address 17, only the memory space of the range is read and the **object** of the writing is **obtained**. Thus, a memory 3B cannot read and rewrite at the program of the ROM 4 and the unfair forging can be prevented.

16/5/21 (Item 21 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2003 JPO & JAPIO. All rts. reserv.

01997688 **Image available**
IC CARD

PUB. NO.: 61-211788 [JP 61211788 A]
PUBLISHED: September 19, 1986 (19860919)
INVENTOR(s): SHINAGAWA TORU
APPLICANT(s): HITACHI MAXELL LTD [000581] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-051594 [JP 8551594]
FILED: March 16, 1985 (19850316)
INTL CLASS: [4] G06K-019/00; G06F-015/30
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 45.4 (INFORMATION PROCESSING -- Computer Applications)
JAPIO KEYWORD: R087 (PRECISION MACHINES -- Automatic Banking)
JOURNAL: Section: P, Section No. 545, Vol. 11, No. 42, Pg. 61, February 06, 1987 (19870206)

ABSTRACT

PURPOSE: To facilitate a mass-production and to improve a generality by providing a **non - volatile memory** storing a processing program writing program, mounting the **non - volatile memory** capable of being electrically erased on a card body, and thereafter writing a processing program therein.

CONSTITUTION: In producing an IC card, in a program memory 3, a processing program writing program is previously written, in an area 8 of a program memory 4, a start address in the memory 3 is stored and mounted on a card body 5 to complete the IC card. After the card is completed, when the card body 5 is mounted to the terminal, by the start address, the processing program writing program is read from the memory 3, a processor 2 operates based on this and performs a writing to the program memory 4 of the processing program inputted from a terminal. At this time, in the area 8, a rewriting of the start address is done. Thereby, a mass-production can be done and in the IC card, any processing program can be written any time, so that a generality is improved.

16/5/25 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015028792 **Image available**
WPI Acc No: 2003-089309/200308
XRPX Acc No: N03-070357

Programmable dedicated application card has RAM and non - volatile memories for software application and control and interfacing

Patent Assignee: GILBERT D A (GILB-I)

Inventor: GILBERT D A

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6457099	B1	20020924	US 9898091	P	19980827	200308 B
			US 99384046	A	19990826	

Priority Applications (No Type Date): US 9898091 P 19980827; US 99384046 A 19990826

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 6457099	B1	18	G06F-013/10	Provisional application US 9898091

Abstract (Basic): US 6457099 B1

NOVELTY - Card comprises a first non - volatile memory (EPROM , EEPROM , Flash RAM , ferroelectric RAM , battery-backed RAM) storing a software application , RAM , a second non - volatile memory , a RISC processor executing the software application, a communication means for the elements, means for seamlessly controlling the card and interfacing its software application with the host computer system and means for translating the host computer system instruction set. The means for controlling and interfacing (host control programme) comprises a means for initialising the card, a means for registering the software application with the host computer system, a means for loading the application for execution and a means for operating the application.

DETAILED DESCRIPTION - There are INDEPENDENT CLAIMS for:

- (1) A host control program for a programmable dedicated application card
- (2) A client interface program for a programmable dedicated application card
- (3) A network administrator program for a server
- (4) A method of operating a software application on a programmable dedicated application card
- (5) A method of manufacturing a programmable dedicated application card

USE - Programmable dedicated application card is for a host computer system.

ADVANTAGE - Card increases execution speed, frees resources and stores the software application in EPROM, so that it cannot be tampered with, and makes upgrading simple.

DESCRIPTION OF DRAWING(S) - The figure shows the control flow of the client interface program software component.

pp; 18 DwgNo 4/9

Title Terms: PROGRAM; DEDICATE; APPLY; CARD; RAM ; NON; VOLATILE; MEMORY; SOFTWARE; APPLY; CONTROL; INTERFACE
Derwent Class: T01; T04; U14
International Patent Class (Main): G06F-013/10
File Segment: EPI

16/5/28 (Item 6 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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014556082 **Image available**

WPI Acc No: 2002-376785/200241

XRPX Acc No: N02-294637

Integrated circuit card includes read-write non - volatile memory which stores program for executing patch program and management information in read only and rewritable memory areas

Patent Assignee: NIPPON TELEGRAPH & TELEPHONE CORP (NITE); NTT ELECTRONIC TECHNOLOGY KK (NITE); TOKIN CORP (TOHM)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2002049904	A	20020215	JP 2000238155	A	20000807	200241 B

Priority Applications (No Type Date): JP 2000238155 A 20000807

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2002049904	A		6 G06K-019/07	

Abstract (Basic): JP 2002049904 A

NOVELTY - The processing program is stored into a read-write non - volatile memory, such that program for executing a patch program is stored into a read only memory area, and the management information is stored into rewritable memory area.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for integrated circuit card mounting processing program modification method.

USE - Integrated circuit (IC) card with read-write non - volatile memory .

ADVANTAGE - Enables continuous usage. Enables modification of information in card without alteration of program.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart explaining the execution of patch program. (Drawing includes non-English language text).

pp; 6 DwgNo 2/3

Title Terms: INTEGRATE; CIRCUIT; CARD; READ; WRITING; NON; VOLATILE; MEMORY ; STORAGE; PROGRAM; EXECUTE; PATCH; PROGRAM; MANAGEMENT; INFORMATION; READ; REWRITING; MEMORY; AREA
Derwent Class: P76; T01; T04
International Patent Class (Main): G06K-019/07
International Patent Class (Additional): B42D-015/10; G06F-001/00; G06K-017/00; G06K-019/10

File Segment: EPI; EngPI

16/5/30 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014360107 **Image available**
WPI Acc No: 2002-180808/200224
XRPX Acc No: N02-137458

Smart card for security and authentication, has memory having
application area for flexibly extending functionality of smart card
and portions compatible with existing smart card systems

Patent Assignee: SCHLUMBERGER SYSTEMES (SLMB)

Inventor: AMARD F

Number of Countries: 026 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1113387	A2	20010704	EP 2000403720	A	20001229	200224 B

Priority Applications (No Type Date): US 99475956 A 19991231

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
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EP 1113387	A2 E	10	G06K-019/073	
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Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT
LI LT LU LV MC MK NL PT RO SE SI TR

Abstract (Basic): EP 1113387 A2

NOVELTY - Memory storing multiple applications is coupled to a processor executing applications. Memory has mapping that includes application areas (420,428) for storing applications and application area (450) for flexibly extending the functionality of smart card. Portions of memory unrelated to extension of functionality are configured to be compatible with existing smart card systems.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for non - volatile memory.

USE - For security and authentication, information storage and retrieval and credit and debit operations for managing value accounts such as prepaid phone time and debit accounts.

ADVANTAGE - Improves flexibility by incorporating new applications without reprogramming the software and reconfiguring hardware of such systems and provides interface that is compatible with existing smart card system.

DESCRIPTION OF DRAWING(S) - The figure shows the memory areas of non - volatile memory.

Application areas (420,428,450)

pp; 10 DwgNo 4/5

Title Terms: SMART; CARD; SECURE; AUTHENTICITY; MEMORY; APPLY; AREA;
FLEXIBLE; EXTEND; FUNCTION; SMART; CARD; PORTION; COMPATIBLE; EXIST;
SMART; CARD; SYSTEM

Derwent Class: T01; T04; T05; U14

International Patent Class (Main): G06K-019/073

File Segment: EPI

16/5/32 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014135076 **Image available**

WPI Acc No: 2001-619287/200172

XRPX Acc No: N01-461822

IC card stores link information about hierarchically maintained files in separate memory

Patent Assignee: TOSHIBA KK (TOKE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2001034512	A	20010209	JP 99209838	A	19990723	200172 B

Priority Applications (No Type Date): JP 99209838 A 19990723

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2001034512	A	11	G06F-012/00	

Abstract (Basic): JP 2001034512 A

NOVELTY - The IC card has a non - volatile memory to store definition information about files maintained in a predefined hierarchy. Another memory stores link information of files specified in non - volatile memory .

USE - For data management in IC card system.

ADVANTAGE - Reduces amount of data stored in memory for managing files .

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of IC card .

pp; 11 DwgNo 2/15

Title Terms: IC; CARD; STORAGE; LINK; INFORMATION; HIERARCHY; MAINTAIN; FILE; SEPARATE; MEMORY

Derwent Class: T01; T04

International Patent Class (Main): G06F-012/00

International Patent Class (Additional): G06K-019/07

File Segment: EPI

16/5/33 (Item 11 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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013978490 **Image available**

WPI Acc No: 2001-462704/200150

Electronic name card

Patent Assignee: CHOI S D (CHOI-I)

Inventor: CHOI S D

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
KR 2001004806	A	20010115	KR 9925527	A	19990624	200150 B

Priority Applications (No Type Date): KR 9925527 A 19990624

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
KR 2001004806	A	1	G06F-015/00	

Abstract (Basic): KR 2001004806 A

NOVELTY - An electronic name card is provided to transmit a name card on communication line and to make a database of name card automatically in a computer.

DETAILED DESCRIPTION - An electronic calling card is operated as follows. When a user clicks on the transmission button to transmit

the contents of his calling card, a microprocessor unit starts the transmission program, and puts an ordinary infrared rays transmission port. Conversely, if the user clicks on the reception button to receive the contents of others' name card, the microprocessor unit starts the reception program. The received data can be stored in a non-volatile memory, and the stored name card constructs a database so that they can be searched by companies, occupations, etc. And the user can see the contents of the stored name card on a screen, and make a telephone call without dialing.

pp; 1 DwgNo 1/10
Title Terms: ELECTRONIC; NAME; CARD
Derwent Class: T01
International Patent Class (Main): G06F-015/00
File Segment: EPI

16/5/37 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013746727 **Image available**
WPI Acc No: 2001-230956/200124
XRPX Acc No: N01-164690

Integrated circuit card for file security mechanism, prevents accessing right of file, when security modification prohibition command is received from exterior

Patent Assignee: DAINIPPON PRINTING CO LTD (NIPQ)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2001034729	A	20010209	JP 99202378	A	19990716	200124 B

Priority Applications (No Type Date): JP 99202378 A 19990716

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2001034729	A		7 G06K-019/073	

Abstract (Basic): JP 2001034729 A

NOVELTY - A flag is provided on management area of each file of IC card non-volatile memory, which shows whether the accessing right of files is alterable or not. The modification of flag is impossible when a security modification prohibition command is received from exterior and thereby the accessing right which modifies the files, is prevented.

USE - For file security mechanism.

ADVANTAGE - Avoids changing accessing right of a file, thereby high security is provided.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of IC card connected with reader-writer apparatus.

pp; 7 DwgNo 1/9

Title Terms: INTEGRATE; CIRCUIT; CARD; FILE; SECURE; MECHANISM; PREVENT; ACCESS; RIGHT; FILE; SECURE; MODIFIED; PROHIBIT; COMMAND; RECEIVE; EXTERIOR

Derwent Class: T01; T04
International Patent Class (Main): G06K-019/073
International Patent Class (Additional): G06F-012/00; G06F-012/14
File Segment: EPI

16/5/40 (Item 18 from file: 350)

DIALOG(R)File 350:Derwent WPIX
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013479378 **Image available**

WPI Acc No: 2000-651321/200063

XRPX Acc No: N00-483000

Semiconductor integrated circuit device transposes address in programmable area of non - volatile memory block to equivalent address in arbitrary programmable area in memory block

Patent Assignee: TOSHIBA KK (TOKE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2000267846	A	20000929	JP 9969930	A	19990316	200063 B

Priority Applications (No Type Date): JP 9969930 A 19990316

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2000267846	A		7 G06F-009/06	

Abstract (Basic): JP 2000267846 A

NOVELTY - A non - volatile memory block (11) has arbitrary programmable area (Po) and predetermined programmable area (P1) limited within specific range. An adder (12) receives address from input terminals (A,B) and transposes address in area (P1) to equivalent address in area (Po). The function of adder is controlled based on program situation in the area (P1).

USE - Semiconductor integrated circuit device with erasable programmable read only memory block for one time program (OTP).

ADVANTAGE - Memory area is not wasted, as program can be reperformed, thereby access of new program can be simplified. Thus optimum semiconductor integrated circuit device is obtained for rescue of OTP product by program correction.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of semiconductor integrated circuit device.

Non - volatile memory block (11)

Adder (12)

Input terminals (A,B)

Programmable areas (Po,P1)

pp; 7 DwgNo 1/7

Title Terms: SEMICONDUCTOR; INTEGRATE; CIRCUIT; DEVICE; TRANSPOSE; ADDRESS; PROGRAM; AREA; NON; VOLATILE; MEMORY; BLOCK; EQUIVALENT; ADDRESS; ARBITRARY; PROGRAM; AREA; MEMORY; BLOCK

Derwent Class: T01

International Patent Class (Main): G06F-009/06

International Patent Class (Additional): G06F-015/78; H01L-021/8247; H01L-029/788; H01L-029/792

File Segment: EPI

16/5/55 (Item 33 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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011631504 **Image available**

WPI Acc No: 1998-048632/199805

XRPX Acc No: N98-038903

IC card with defective memory detection function - has processing unit which performs diagnostic process for first and second memories and recoverability process for second memory based on instruction received

through communication unit

Patent Assignee: TOPPAN PRINTING CO LTD (TOPP)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 9297830	A	19971118	JP 96110913	A	19960501	199805 B

Priority Applications (No Type Date): JP 96110913 A 19960501

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 9297830	A	8	G06K-019/07	

Abstract (Basic): JP 9297830 A

The IC card has a first non-volatile memory (2) which stores program and a second non-volatile memory (4) which stores data. A communication unit sends and receives data from external apparatus. Based on the program stored in the first non-volatile memory, the instruction which is received via communication unit is executed.

A processing unit transmits execution result to external apparatus via communication part and the processing unit performs diagnostic process for first and second memories and recoverability process for second memory based on instruction received.

ADVANTAGE - Shortens processing time. Suppresses influence which affects sensor.

Dwg.1/9

Title Terms: IC; CARD; DEFECT; MEMORY; DETECT; FUNCTION; PROCESS; UNIT; PERFORMANCE; DIAGNOSE; PROCESS; FIRST; SECOND; MEMORY; PROCESS; SECOND; MEMORY; BASED; INSTRUCTION; RECEIVE; THROUGH; COMMUNICATE; UNIT

Derwent Class: T01; T04

International Patent Class (Main): G06K-019/07

International Patent Class (Additional): G06F-011/22; G06F-012/16

File Segment: EPI

16/5/57 (Item 35 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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011565063 **Image available**

WPI Acc No: 1997-541544/199750

XRPX Acc No: N97-450878

Portable data memory medium e.g. integrated circuit card - has data management unit that approves access to data area in non-volatile memory when application data are in accord with access condition data

Patent Assignee: DAINIPPON PRINTING CO LTD (NIPQ)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 9259235	A	19971003	JP 9662985	A	19960319	199750 B

Priority Applications (No Type Date): JP 9662985 A 19960319

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 9259235	A	9	G06K-017/00	

Abstract (Basic): JP 9259235 A

The memory medium includes an external communication unit (11) and a data management unit (12). A non-volatile memory (15) has a

data area provided with an access condition preservation area where data are stored.

A person applying for access to the data area is identified by obtaining an applicant data through the communication unit. The **application** data are compared with **access** condition data. The data management unit approves the access to the data area when the compared data corresponds with each other.

ADVANTAGE - Does not need to input applicant data for every transaction. Does not need to undergo complicated procedure. Prevents unauthorised person from obtaining applicant data since applicant data are not entered to transaction terminal.

Dwg.1/7

Title Terms: PORTABLE; DATA; MEMORY; MEDIUM; INTEGRATE; CIRCUIT; CARD; DATA ; MANAGEMENT; UNIT; ACCESS; DATA; AREA; MEMORY; APPLY; DATA; ACCORD;

ACCESS; CONDITION; DATA

Index Terms/Additional Words: IC

Derwent Class: T01; T04

International Patent Class (Main): G06K-017/00

International Patent Class (Additional): G06F-017/60; G06K-019/073

File Segment: EPI

16/5/59 (Item 37 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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011505735 **Image available**

WPI Acc No: 1997-483649/199745

XRPX Acc No: N97-403108

IC card with memory block division flexibility - has third controller which controls writing-in of data into recording memory area or reading-out address, based on data stored in file structure memory area

Patent Assignee: CITIZEN WATCH CO LTD (CITL)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 7306921	A	19951121	JP 8670355	A	19860328	199745 B
			JP 95124647	A	19860328	

Priority Applications (No Type Date): JP 8670355 A 19860328; JP 95124647 A 19860328

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7306921	A		13	G06K-019/07	Div ex application JP 8670355

Abstract (Basic): JP 7306921 A

The card has a **non - volatile** solid state **memory** and a first **memory** which **stores** a set of **files** . The writing-in/reading-out of data to/from the first memory is controlled by a data processing controller. A **file structure memory** area includes a **record size memory** area and a **record reservation number memory** area for storing the information relevant to the **stored files** . A processing controller writes-in the record size and reservation number to the **file structure memory** area, using a **file reservation part**, based on the file structure designation data input from external.

A second controller controls the open state of a designated file. A third controller controls the writing-in of data to a **record data memory** area or reading-out of address, based on the data **stored** in the **file structure memory** area, in response to the read/write

instruction received during file open state.

ADVANTAGE - Enables to perform block division of memory flexibly.
Simplifies data accessing. Enables to establish size and number of
records of each file.

Dwg.1/10

Title Terms: IC; CARD; MEMORY; BLOCK; DIVIDE; FLEXIBLE; THIRD; CONTROL;
CONTROL; WRITING; DATA; RECORD; MEMORY; AREA; READ; ADDRESS; BASED; DATA;
STORAGE; FILE; STRUCTURE; MEMORY; AREA

Index Terms/Additional Words: COMPUTER

Derwent Class: T01; T04

International Patent Class (Main): G06K-019/07

File Segment: EPI

16/5/63 (Item 41 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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009887811 **Image available**

WPI Acc No: 1994-167726/199420

Related WPI Acc No: 2001-069797

XRPX Acc No: N94-131965

Host and user transaction system of self-contained portable intelligence
appts. - has integrated circuit card incorporating single chip
microcomputer with I-O communication, non - volatile and random
access memory

Patent Assignee: INTELLECT AUSTRALIA PTY LTD (INTE-N)

Inventor: BERTINA J M G; OLIVER R Q; OLIVER Q R

Number of Countries: 023 Number of Patents: 010

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9410657	A1	19940511	WO 93AU552	A	19931026	199420 B
AU 9453321	A	19940524	WO 93AU552	A	19931026	199434
			AU 9453321	A	19931026	
NO 9501575	A	19950626	WO 93AU552	A	19931026	199535
			NO 951575	A	19950425	
EP 706692	A1	19960417	EP 93923424	A	19931026	199620
			WO 93AU552	A	19931026	
US 5682027	A	19971028	WO 93AU552	A	19931026	199749
			US 95424258	A	19950620	
AU 687760	B	19980305	AU 9453321	A	19931026	199820
AU 9748344	A	19980219	AU 9453321	A	19931026	199824 N
			AU 9748344	A	19971210	
AU 700628	B	19990107	AU 9453321	A	19931026	199913 N
			AU 9748344	A	19971210	
US 6091817	A	20000718	WO 93AU552	A	19931026	200037
			US 95424258	A	19950620	
			US 97957722	A	19971024	
US 6095412	A	20000801	WO 93AU552	A	19931026	200039
			US 95424258	A	19950620	
			US 97957714	A	19971024	

Priority Applications (No Type Date): AU 925520 A 19921026; AU 9748344 A
19971210

Cited Patents: EP 427465; US 4831242; US 4926480; WO 9117524

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

WO 9410657 A1 E 57 G06K-019/073

Designated States (National): AU CA JP KR NO US

Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL
PT SE

AU 9453321 A G06K-019/073 Based on patent WO 9410657
 NO 9501575 A G06K-019/07
 EP 706692 A1 E 57 G06K-019/073 Based on patent WO 9410657
 Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LI LU MC
 NL PT SE
 US 5682027 A 21 G06K-005/00 Based on patent WO 9410657
 AU 687760 B G06K-019/073 Previous Publ. patent AU 9453321
 Based on patent WO 9410657
 AU 9748344 A G06K-019/073 Div ex application AU 9453321
 AU 700628 B G06K-019/073 Div ex application AU 9453321
 Previous Publ. patent AU 9748344
 US 6091817 A H04L-009/00 Cont of application WO 93AU552
 Cont of application US 95424258
 US 6095412 A G06K-005/00 Cont of application WO 93AU552
 Cont of application US 95424258

Abstract (Basic): WO 9410657 A

The system has an interface device (11) with its own memory for storing data and a coupler (14) to connect to the IC card. The nonvolatile memory (17,19) has an operating system mask programmed in native code for performing basic functions and a second part has data files into different access restriction levels.

The random access memory is used by the operating system and for storing data received from or ready for transmission via the communication port. The interface device has a programme module with one or more instructions and the operating system has a command executor and programme interpreter.

USE - Host and user transaction system for commercial transactions using several users and several service providers.

Dwg.2/9

Title Terms: HOST; USER; TRANSACTION; SYSTEM; SELF; CONTAIN; PORTABLE; INTELLIGENCE; APPARATUS; INTEGRATE; CIRCUIT; CARD; INCORPORATE; SINGLE; CHIP; MICROCOMPUTER; I-O; COMMUNICATE; NON; VOLATILE; RANDOM; ACCESS; MEMORY

Index Terms/Additional Words: COMMERCIAL

Derwent Class: P76; T01; T04

International Patent Class (Main): G06K-005/00; G06K-019/07; G06K-019/073; H04L-009/00

International Patent Class (Additional): B42D-015/10; G06F-017/60

File Segment: EPI; EngPI

16/5/71 (Item 49 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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008505898 **Image available**

WPI Acc No: 1991-009982/199102

XRFX Acc No: N91-007774

Integrated circuit with programmable circuit - uses volatile memory disposed in programmable circuit on a chip for storing program data concerning the programmable circuit

Patent Assignee: KAWASAKI STEEL CORP (KAWI)

Inventor: SAKAMOTO M

Number of Countries: 006 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 406996	A	19910109	EP 90301784	A	19900220	199102 B
CA 2010122	A	19901221				199111
US 5058074	A	19911015	US 90480890	A	19900216	199144

Priority Applications (No Type Date): JP 89159293 A 19890621
Cited Patents: 1.Jnl.Ref; EP 238230; EP 307912; EP 55348; US 4761647
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
EP 406996 A
Designated States (Regional): DE FR GB NL

Abstract (Basic): EP 406996 A

The **integrated circuit** comprises a **volatile memory** (2) disposed in a programmable circuit (1) on a chip for **storing program data** concerning the programmable circuit. A **non - volatile memory** (3) is disposed externally of the programmable circuit permitting the program data to be written from the outside (4). The **program data** written in the **non - volatile memory** or **program data** supplied from a terminal (5) provided outside the **volatile memory** is transmitted.

The transferring circuit comprises a clock (41), a frequency divider (42) and a counter (43) for the clock divisions. An address is generated synchronised with the clock. The address is decoded as a read address to select a word line for both memories.

ADVANTAGE - Provides handy and economical **integrated circuit** capable of improved degree of integration and easing alteration of program data upon circuit evaluation. (7pp Dwg.No.1/3)

Title Terms: INTEGRATE; CIRCUIT; PROGRAM; CIRCUIT; VOLATILE; MEMORY; DISPOSABLE; PROGRAM; CIRCUIT; CHIP; STORAGE; PROGRAM; DATA; PROGRAM; CIRCUIT

Derwent Class: T01; U13; U14; U21

International Patent Class (Additional): G06F-013/00; G06F-015/46;

G11C-007/00; G11C-014/00; G11C-016/06; G11C-029/00; H03K-019/01

File Segment: EPI

16/5/75 (Item 53 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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007697849 **Image available**

WPI Acc No: 1988-331781/198847

XRPX Acc No: N88-251465

High reliability, increased processing speed IC card - transfers processing program and data necessary for current processing, from non volatile memory to memory of shorter access time

Patent Assignee: HITACHI MAXELL KK (HITM)

Inventor: MIYAMOTO K; SHINAGAWA T; SUGAWARA K; YAMAUCHI S

Number of Countries: 003 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 292237	A	19881123	EP 88304457	A	19880517	198847 B
EP 292237	B1	19950208	EP 88304457	A	19880517	199510
DE 3852965	G	19950323	DE 3852965	A	19880517	199517
			EP 88304457	A	19880517	
EP 292237	B2	20000301	EP 88304457	A	19880517	200016

Priority Applications (No Type Date): JP 87122289 A 19870519; JP 87122288 A 19870519

Cited Patents: 1.Jnl.Ref; A3...9017; EP 167044; EP 77404; JP 61060131;

No-SR.Pub; WO 8000383; EP 220718; WO 800383

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

EP 292237 A E 10

Designated States (Regional): DE FR GB
EP 292237 B2 E G06F-015/76
Designated States (Regional): DE FR GB
EP 292237 B1 E 15 G06F-015/76
Designated States (Regional): DE FR GB
DE 3852965 G G06F-015/76 Based on patent EP 292237

Abstract (Basic): EP 292237 A

The IC card (5) comprises an operation/processing unit (1) and a non - volatile storage device (3) for storing processing programs or data to be executed by the processing unit. A second storage device (4) is provided having a shorter access time than the first device. The processing unit transfers the processing programs in the first store to the second store, accesses the second store to fetch the programs or data and responds to an external signal.

The processing unit has as the last program a data return processing for transferring data stored in the second device to a data area standing for the original position of that data within the first storage device

Title Terms: HIGH; RELIABILITY; INCREASE; PROCESS; SPEED; IC; CARD; TRANSFER; PROCESS; PROGRAM; DATA; NECESSARY; CURRENT; PROCESS; NON; VOLATILE; MEMORY; MEMORY; SHORT; ACCESS; TIME

Derwent Class: T01; T04

International Patent Class (Main): G06F-015/76

International Patent Class (Additional): G06F-015/06

File Segment: EPI

16/5/76 (Item 54 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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007535706

WPI Acc No: 1988-169638/198825

XPX Acc No: N88-129740

Storage of computer program supplied to user - uses external integrated circuit to hold correct versions of sub-programs which are called from program as it is executed

Patent Assignee: EUROTECHNIQUE SA (EURO-N)

Inventor: LISIMAQUE G

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
FR 2606185	A	19880506	FR 8615324	A	19861104	198825 B

Priority Applications (No Type Date): FR 8615324 A 19861104

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
FR 2606185	A	10		

Abstract (Basic): FR 2606185 A

The user program is supplied as a set of programs and sub- programs which are loaded into the memory of a computer. The sub- programs in memory are incomplete, and the completed version of the sub- programs is stored in non - volatile memory incorporated in an integrated circuit external to the computer. The memory can only be read when suitable signals are provided from the computer.

If an unauthorised user runs the program the incomplete sub-programs are invoked, while for an authorised user the complete sub- programs from the external memory are called.

USE/ADVANTAGE - Copying protection for computer programs, requiring hardware attachment to allow full version of program to run.

0/1

Title Terms: STORAGE; COMPUTER; PROGRAM; SUPPLY; USER; EXTERNAL; INTEGRATE; CIRCUIT; HOLD; CORRECT; VERSION; SUB; PROGRAM; CALL; PROGRAM; EXECUTE

Index Terms/Additional Words: STORAGE; COMP

Derwent Class: T01

International Patent Class (Additional): G06F-012/14; G06K-019/02

File Segment: EPI

16/5/77 (Item 55 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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007416138 **Image available**

WPI Acc No: 1988-050073/198807

XRPX Acc No: N88-037958

Volatile-nonvolatile integrated circuit configured with CAD system - has two sections interconnected so that data can be entered in non-volatile memory transferred at HF voltage segment to recall data

Patent Assignee: NCR CORP (NATC)

Inventor: TOPICH J A

Number of Countries: 005 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8801095	A	19880211	WO 87US1673	A	19870720	198807	B
US 4754432	A	19880628	US 86889543	A	19860725	198828	
EP 275286	A	19880727	EP 87904792	A	19870720	198830	
JP 1500381	W	19890209	JP 87504168	A	19870720	198912	
EP 275286	B	19911121				199147	
DE 3774683	G	19920102				199202	

Priority Applications (No Type Date): US 86889543 A 19860725

Cited Patents: 1.Jnl.Ref; No-SR.Pub; US 4138737

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

WO 8801095 A E 20

Designated States (National): JP

Designated States (Regional): DE GB NL

US 4754432 A 11

EP 275286 A E

Designated States (Regional): DE GB NL

EP 275286 B

Designated States (Regional): DE GB NL

Abstract (Basic): WO 8801095 A

The volatile/nonvolatile circuit has a volatile shift register stage (2) having data input, data output, and clocking lines (7, 8, 11), and a nonvolatile storage (3) coupled to the volatile shift register stage. The nonvolatile storage is responsive to a selective program command to store the binary state in the volatile shift register stage.

A recall device (19) connected to the register stage and to the non-volatile storage is responsive to a selective recall command to set the register stage to the binary state stored in the nonvolatile storage. The latter includes a field effect device configured with a single polysilicon electrode layer.

USE - Trimming ladder networks, coding and decoding of encrypted data, setting of filter breakpoints, gain characteristics etc.

1/8

Title Terms: VOLATILE; INTEGRATE; CIRCUIT; CONFIGURATION; CAD; SYSTEM; TWO;
SECTION; INTERCONNECT; SO; DATA; CAN; ENTER; NON; VOLATILE; MEMORY;
TRANSFER; HF; VOLTAGE; SEGMENT; RECALL; DATA
Index Terms/Additional Words: DIP
Derwent Class: U13; U14; U21
International Patent Class (Additional): G11C-011/00; G11C-014/00;
G11C-019/00
File Segment: EPI

16/5/78 (Item 56 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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007102655

WPI Acc No: 1987-102652/198715

XRPX Acc No: N87-077199

Smart card with memory divided into system and user program areas
- has correspondence table between newly added function code and start
address of added function program

Patent Assignee: TOSHIBA KK (TOKE)

Inventor: HIROKAWA K; IIJIMA Y

Number of Countries: 004 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 218176	A	19870415	EP 86113432	A	19860930	198715 B
US 4827512	A	19890502	US 86915514	A	19860106	198920
EP 218176	B	19911113				199146
DE 3682476	G	19911219				199201

Priority Applications (No Type Date): JP 86150432 A 19860626; JP 85223112 A
19851007; JP 86114151 A 19860519

Cited Patents: 2.Jnl.Ref; A3...8837; EP 152024; EP 57602; EP 89876; JP
60153582; No-SR.Pub

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing	Notes
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EP 218176	A	E	22			
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Designated States (Regional): DE FR GB

US 4827512	A		20			
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EP 218176	B					
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Designated States (Regional): DE FR GB

Abstract (Basic): EP 218176 A

A text transmitted between the IC card and a host system connected to it includes a command text and a response text. Either text includes a flag indicating that the text is written in the user program or system program area of the memory area. The latter has a conversion table for a function code and the start address of a program corresp. to the function code.

The conversion table is looked up by using the given function code as a parameter, thus obtaining the start address of the corresp. program. The memory area has a correspondence table between a newly added function code and the start address of an added function program. The latter is selectively executed.

USE/ADVANTAGE - Reads, writes or erases data w.r.t. incorporated data memory by internal control element. Can store and execute new function program in addition to already stored function programs.

4, 5/24

Title Terms: SMART; CARD; MEMORY; DIVIDE; SYSTEM; USER; PROGRAM; AREA;

CORRESPOND; TABLE; NEW; ADD; FUNCTION; CODE; START; ADDRESS; ADD;
FUNCTION; PROGRAM
Derwent Class: T01; T04
International Patent Class (Additional): G06F-009/26; G06K-005/00;
G07F-007/10; H04L-009/00
File Segment: EPI

16/5/79 (Item 57 from file: 350)
DIALOG(R) File 350: Derwent WPIX
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003011911

WPI Acc No: 1981-B1920D/198106

NC appts. with magnetic, integrated circuit bubble memory - transfers
memory content to interfacing, fast access memory directly
accessible by processor

Patent Assignee: FUJITSU FANUC LTD (FUFA); IMAZEKI R (IMAZ-I)

Inventor: KURAKAKE M

Number of Countries: 005 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 8100158	A	19810122				198106 B
EP 30981	A	19810701	EP 80901219	A	19800630	198128
US 4589091	A	19860513	US 81572137	A	19810220	198622
EP 30981	B	19871028				198743
DE 3072047	G	19871203				198749

Priority Applications (No Type Date): JP 79U90562 U 19790630

Cited Patents: 1.Jnl.Ref; DE 2742124; FR 2356985; JP 48028892; JP 54042578

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

WO 8100158 A J

Designated States (National): SU US

Designated States (Regional): DE FR GB

EP 30981 A E

Designated States (Regional): DE FR GB

EP 30981 B E

Designated States (Regional): DE FR GB

Abstract (Basic): WO 8100158 A

Numerical control appts. using a large-capacity, non - volatile
magnetic bubble memory (1) storing instructions, e.g., machining
instructions, for a processor (3) includes a high-speed access,
volatile integrated circuit memory (2) which connects directly
to the processor (3) and through an interface (4) to the bubble memory
(1).

On arrival of a power-on signal (PON), an element or section (1a)
is supplied, by a read-write control circuit (1b) in the bubble memory,
through the interface (4) to the high-speed memory (2), which can then
be accessed for information by the processor (3). If the high-speed
memory capacity is small, this action can be repeated during
processing..

Equipment is still cheap, but action is faster than when the bubble
memory is accessed directly by a processor

Title Terms: NC; APPARATUS; MAGNETIC; INTEGRATE; CIRCUIT; BUBBLE; MEMORY;
TRANSFER; MEMORY; CONTENT; INTERFACE; FAST; ACCESS; MEMORY; ACCESS;
PROCESSOR

Index Terms/Additional Words: NUMERIC; CONTROL

Derwent Class: T06; X25

International Patent Class (Additional): G05B-019/40; G06F-007/00;

17/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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06570050 **Image available**
IC CARD

PUB. NO.: 2000-155819 [JP 2000155819 A]
PUBLISHED: June 06, 2000 (20000606)
INVENTOR(s): YOSHIKAWA MASAKI
APPLICANT(s): DAINIPPON PRINTING CO LTD
APPL. NO.: 10-347803 [JP 98347803]
FILED: November 20, 1998 (19981120)
INTL CLASS: G06K-019/07

ABSTRACT

PROBLEM TO BE SOLVED: To ensure ever perfect security.

SOLUTION: Relating to an IC card in which a CPU 11, a ROM 13, an EEPROM 14 and a RAM 15 are incorporated, plural application programs are stored in the EEPROM 14 so as to be enciphered by using enciphering methods different for each block 51, 52, 61, and 62. Deciphering procedures AA, BB and CC corresponding to those enciphering methods are prepared in the ROM 13. When it is necessary to execute a specific application, the application program is deciphered, and the deciphered program is developed in the RAM 15, and the developed program is executed. At the time of ending the application program, the program developed in the RAM 15 is deleted.

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17/5/3 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO
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06563201 **Image available**
IC CARD

PUB. NO.: 2000-148944 [JP 2000148944 A]
PUBLISHED: May 30, 2000 (20000530)
INVENTOR(s): WAKAMATSU MASAKI
APPLICANT(s): DAINIPPON PRINTING CO LTD
APPL. NO.: 10-342339 [JP 98342339]
FILED: November 16, 1998 (19981116)
INTL CLASS: G06K-019/07

ABSTRACT

PROBLEM TO BE SOLVED: To deal with an application program described in plural languages and to recognize a correspondent language from the outside.

SOLUTION: In an IC card 10 having a CPU 11, a ROM 13, an EEPROM 14 and a RAM 15, plural interpreter programs are stored in the ROM 13, and an optical program can be made to be loaded from an external device 20 in the EEPROM 14. When a loaded application program is carried out, an interpreter program corresponding to the description language of the program is selected in the ROM 13 and is carried out. When a response signal (ATR sign) is returned to a reset signal from the device 20, information showing the correspondent language of a built-in interpreter is

included in the response signal and the correspondent language is imparted to the device 20.

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17/5/4 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO
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06178761 **Image available**
IC CARD AND IC CARD READER

PUB. NO.: 11-120310 [JP 11120310 A]
PUBLISHED: April 30, 1999 (19990430)
INVENTOR(s): IKEDA YOSHIHIRO
APPLICANT(s): TAMURA ELECTRIC WORKS LTD
APPL. NO.: 09-282138 [JP 97282138]
FILED: October 15, 1997 (19971015)
INTL CLASS: G06K-017/00; G06F-019/00

ABSTRACT

PROBLEM TO BE SOLVED: To prevent a rechargeable type IC card from illegally being used by providing a nonvolatile memory with a charge amount area where a value charged in a value area is stored as a charge amount and a unique number area where a unique number added to the value is stored.

SOLUTION: An IC card 1 consists of a CPU 11, a memory 12 storing a program, etc., an external interface 13 as an interface between a store terminal 2 and a charge terminal 4, and a nonvolatile RAM 14. The nonvolatile RAM 14 is provided with a unique number area 14A where the unique number (n) of the IC card is stored, a charge amount area 14B where a charge amount M changed for the IC card 1 is stored and a value area 14C where the balance of the IC card 1 is stored as a value V1. Then, when an article is purchased, the IC card 1 transmits the unique number (n), the charge amount M and an amount to be used to the store terminal 2 and stores the amount obtained by subtracting the amount to be used from the value V1 in the value area 14C.

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17/5/6 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO
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06097679 **Image available**
IC CARD

PUB. NO.: 11-039198 [JP 11039198 A]
PUBLISHED: February 12, 1999 (19990212)
INVENTOR(s): HAYASHI MASAHIRO
IRISAWA KAZUYOSHI
APPLICANT(s): DAINIPPON PRINTING CO LTD
APPL. NO.: 09-192386 [JP 97192386]
FILED: July 17, 1997 (19970717)
INTL CLASS: G06F-011/34; G06K-019/07

ABSTRACT

PROBLEM TO BE SOLVED: To output in which area of memory a processing error occurs by outputting area information of the memory to which access is made at a processing step in which the error occurs when the processing error occurs in one of the processing steps during execution of an instruction consisting of plural processing steps.

SOLUTION: For example, a processing process 1 is instructed, the access is made to a file F2 of EEPROM and its specified record is read by a CPU. Next, the access is made to a file Fi and its specified record is similarly read and next, a required processing is executed by using work areas WKj, Wkm of RAM. And a specified record of a file Fn of the EEPROM is updated by the processing result. In this case, when each step of the processing process is completed, an incorporated counter is made incremental by the CPU. Therefore, when the error is supposed to occur at a certain processing step, a value to represent contents of the counter at the time is outputted.

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17/5/7 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO
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05841539 **Image available**
IC CARD

PUB. NO.: 10-124639 [JP 10124639 A]
PUBLISHED: May 15, 1998 (19980515)
INVENTOR(s): TAKAHASHI TAKEHIRO
APPLICANT(s): HITACHI MAXELL LTD [000581] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-299883 [JP 96299883]
FILED: October 25, 1996 (19961025)
INTL CLASS: [6] G06K-019/07; G06F-009/06; G06K-017/00
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessors)

ABSTRACT

PROBLEM TO BE SOLVED: To reduce the load of IC card checking processing to a terminal equipment by selecting an application program to be executed by referring to a flag and successively updating the contents of the flag in each reception of a reset signal from the terminal equipment or in each turning-on of a power supply for an IC card.

SOLUTION: An IC card 1 has a processor 2, a ROM 3 for storing a system program, a RAM 4 to be a working area, an EEPROM 5 to be a data storage area, and an I/O port 6 and these elements are mutually connected through a bus 7. An application program to be executed is selected by referring to a flag and the contents of the flag are updated in each reception of a reset signal from a terminal equipment or in each turning-on of the power supply for the card 1. When the card 1 is loaded to the terminal equipment and the power supply is turned on or a reset signal is received from the terminal equipment, the flag is updated to the application program to be executed next.

17/5/11 (Item 11 from file: 347)

DIALOG(R)File 347:JAPIO
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04517776 **Image available**
IC CARD

PUB. NO.: 06-161676 [JP 6161676 A]
PUBLISHED: June 10, 1994 (19940610)
INVENTOR(s): IRISAWA KAZUYOSHI
 HARIMA HIROTSUGU
 JO TERUAKI
APPLICANT(s): DAINIPPON PRINTING CO LTD [000289] (A Japanese Company or
 Corporation), JP (Japan)
APPL. NO.: 04-339611 [JP 92339611]
FILED: November 26, 1992 (19921126)
INTL CLASS: [5] G06F-003/08; G06F-012/02; G06K-019/07
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 30.1
 (MISCELLANEOUS GOODS -- Office Supplies); 45.2 (INFORMATION
 PROCESSING -- Memory Units)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers &
 Microprocessors)
JOURNAL: Section: P, Section No. 1798, Vol. 18, No. 484, Pg. 141,
 September 08, 1994 (19940908)
 ABSTRACT
PURPOSE: To quicken the writing/rewriting processings of a record to
 EEPROM .

CONSTITUTION: In a state where records 1 to 4 are written into **EEPROM** 14,
a DRAW pointer showing a leading address (e) into which a next record
should be written is prepared in a control data area within **EEPROM** .. In
the case of writing a fifth record 5, it is written from an address shown
by the DRAW pointer. Whenever the record is direct-read-after-written, the
content of the DRAW pointer is updated. On the other hand, in the case of
rewriting the plural records 2 to 4 which are continuously recorded, the
address (b) of the record 2 is calculated first and the address (b) is
shown by a rewriting pointer prepared within **RAM** 13. Concerning the
records 3 and 4 to be rewriting **objects** , addresses are **obtained** based
on the rewriting pointer.

17/5/12 (Item 12 from file: 347)
DIALOG(R)File 347:JAPIO
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04408019 **Image available**
IC MEMORY CARD

PUB. NO.: 06-051919 [JP 6051919 A]
PUBLISHED: February 25, 1994 (19940225)
INVENTOR(s): ISHIDOSHIRO TAKASHI
APPLICANT(s): MELCO KK [000000] (A Japanese Company or Corporation), JP
 (Japan)
APPL. NO.: 04-223314 [JP 92223314]
FILED: July 29, 1992 (19920729)
INTL CLASS: [5] G06F-003/08; G06F-003/06
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 30.1
 (MISCELLANEOUS GOODS -- Office Supplies)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers &
 Microprocessors)
JOURNAL: Section: P, Section No. 1746, Vol. 18, No. 287, Pg. 55, May
 31, 1994 (19940531)

ABSTRACT

PURPOSE: To mix a ROM and a RAM in the IC memory card and to use this card as a single filing system.

CONSTITUTION: Managing information CAo of data stored in the IC memory card is stored in the leading area of the ROM. When performing the write of a file, an area to store the managing information of the file is secured on the RAM, and a table LUT to translate the address of access to the managing information of the file is prepared on the RAM. When the file in the IC memory card is accessed later, a computer reads the file managing information CAo and when the file exists on the RAM, however, the address is translated by the translation table LUT so as to read managing information CAa for RAM on the RAM. Therefore, the file of the ROM and the file of the RAM are accessed from the computer side without any distinction.

17/5/14 (Item 14 from file: 347)

DIALOG(R)File 347:JAPIO

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04159669 **Image available**

INTEGRATED CIRCUIT

PUB. NO.: 05-151369 [JP 5151369 A]

PUBLISHED: June 18, 1993 (19930618)

INVENTOR(s): NARITA YOSHINORI

APPLICANT(s): NIPPON STEEL CORP [000665] (A Japanese Company or Corporation), JP (Japan)

APPL. NO.: 03-045331 [JP 9145331]

FILED: February 19, 1991 (19910219)

INTL CLASS: [5] G06F-015/78; G06F-009/22

JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)

JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessors)

JOURNAL: Section: P, Section No. 1623, Vol. 17, No. 546, Pg. 140, September 30, 1993 (19930930)

ABSTRACT

PURPOSE: To provide a one-chip microcomputer which is characterized by a high speed execution of a program, change facility of the program and a simple circuit configuration.

CONSTITUTION: The one-chip microcomputer is loaded with a ROM 13 in which a program for transferring an instruction code to a built-in high speed RAM from an external storage device is stored, a high speed RAM 14 for storing the instruction code and an external storage interface 12. Before the program is executed, a processor 11 of the one-chip microcomputer executes a transfer program and transfers the instruction code on the external storage device 2 to the built-in high speed RAM 14. After the transfer is finished, the processor 11 accesses the built-in high speed RAM 14 and executes the program at a high speed.

17/5/16 (Item 16 from file: 347)

DIALOG(R)File 347:JAPIO

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03988974 **Image available**
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUB. NO.: 04-354074 [JP 4354074 A]
PUBLISHED: December 08, 1992 (19921208)
INVENTOR(s): TANAKA MASAHIRO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP
 (Japan)
 FUJITSU VLSI LTD [491219] (A Japanese Company or Corporation)
 , JP (Japan)
APPL. NO.: 03-129822 [JP 91129822]
FILED: May 31, 1991 (19910531)
INTL CLASS: [5] G06F-015/78
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications)
JAPIO KEYWORD: R129 (ELECTRONIC MATERIALS -- Super High Density **Integrated**
 Circuits , LSI & GS; R131 (INFORMATION PROCESSING --
 Microcomputers & Microprocessors
JOURNAL: Section: P, Section No. 1529, Vol. 17, No. 220, Pg. 98, April
 30, 1993 (19930430)

ABSTRACT

PURPOSE: To develop plural kinds of semiconductor **integrated circuit** devices in a short time by turning some of functional blocks provided in plural numbers into an operating state in respect of an LSI in which a central processing unit, a **ROM** , and a **RAM** are formed on one semiconductor chip.

CONSTITUTION: The CPU 3, the **ROM** 4, the **RAM** 5, a timer 6, a PWM 7, a serial/parallel converter 8, a transferring register 9, and an address decoder 10, etc., are formed on one semiconductor chip 2. The CPU 3 executes a **program** , and the ROM 4 **stores** the **program** the CPU 3 executes. The **RAM** 5 stores data to be used for the execution of the program or an arithmetically operated result. The address decoder 10 decodes an address signal outputted from the CPU 3, and turns some functional blocks among the timer, the PWM 7, the serial/parallel converter 8 and the transferring register 9 into the operating state.

17/5/17 (Item 17 from file: 347)
DIALOG(R)File 347:JAPIO
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02630990 **Image available**
IC CARD

PUB. NO.: 63-247890 [JP 63247890 A]
PUBLISHED: October 14, 1988 (19881014)
INVENTOR(s): KATOU AKIROU
APPLICANT(s): CANON INC [000100] (A Japanese Company or Corporation), JP
 (Japan)
APPL. NO.: 62-080898 [JP 8780898]
FILED: April 03, 1987 (19870403)
INTL CLASS: [4] G06K-019/00; B42D-015/02
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 29.4
 (PRECISION INSTRUMENTS -- Business Machines); 30.9
 (MISCELLANEOUS GOODS -- Other)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers &
 Microprocessors)
JOURNAL: Section: P, Section No. 825, Vol. 13, No. 57, Pg. 131,
 February 09, 1989 (19890209)

ABSTRACT

PURPOSE: To prevent break of elements, destruction of information, or the like by detecting the temperature of circuit elements constituting an information processing circuit and controlling the operation of this circuit in accordance with the detected temperature.

CONSTITUTION: A ROM 2 where a control program is stored and a RAM 3 used as a data storage area are connected to a CPU 1 through a bus line 4. The CPU 1, the ROM 2, and the RAM 3 consist of a one-chip IC, and a temperature detecting circuit 6 which detects the temperature of this IC chip is provided. The operation of the CPU 1 is controlled in accordance with the state detected by the temperature detecting circuit 6.

17/5/18 (Item 18 from file: 347)
DIALOG(R)File 347:JAPIO
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02630989 **Image available**
IC CARD

PUB. NO.: 63-247889 [JP 63247889 A]
PUBLISHED: October 14, 1988 (19881014)
INVENTOR(s): KATO A KIROU
APPLICANT(s): CANON INC [000100] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 62-080897 [JP 8780897]
FILED: April 03, 1987 (19870403)
INTL CLASS: [4] G06K-019/00; B42D-015/02
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 29.4
(PRECISION INSTRUMENTS -- Business Machines); 30.9
(MISCELLANEOUS GOODS -- Other)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers &
Microprocessors)
JOURNAL: Section: P, Section No. 825, Vol. 13, No. 57, Pg. 131,
February 09, 1989 (19890209)

ABSTRACT

PURPOSE: To safely operate an IC card without destruction of stored data, damage of an internal circuit, or the like by controlling feed to an information processing circuit.

CONSTITUTION: A ROM 2 where a control program is stored and a RAM 3 used as a data storage area are connected to a CPU 1 through a bus line 4. A supply voltage is supplied through an electrode 5 of a connector. A current control circuit 6 as the circuit which controls feed to the CPU 1, the ROM 2, and the RAM 3 is connected between the electrode 5 and a power line 7 connected to the CPU 1, the ROM 2, and the RAM 3.

17/5/19 (Item 19 from file: 347)
DIALOG(R)File 347:JAPIO
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02237263 **Image available**
HYBRID INTEGRATED CIRCUIT DEVICE

PUB. NO.: 62-154163 [JP 62154163 A]
PUBLISHED: July 09, 1987 (19870709)

INVENTOR(s): KAGEYAMA SEIICHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 60-295710 [JP 85295710]
FILED: December 27, 1985 (19851227)
INTL CLASS: [4] G06F-015/06; G06F-012/06
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 45.2
(INFORMATION PROCESSING -- Memory Units)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers &
Microprocessors)
JOURNAL: Section: P, Section No. 648, Vol. 11, No. 389, Pg. 85,
December 19, 1987 (19871219)

ABSTRACT

PURPOSE: To secure the easy input of a program for control of a microprocessor IC1 from the outside to this IC1 by connecting a signal output terminal that actuates a **nonvolatile program memory** element IC2 of the IC1 set within a hybrid **integrated circuit** device and an input terminal of the IC2 for the output signal sent from the IC1 to an external terminal respectively and at the same time avoiding the connection between said output and input terminals and an input/output terminal within a package.

CONSTITUTION: An address signal input terminal A15 of an IC1 is connected to an external terminal and also to a chip-enable input terminal, the inverse of CE of an IC3 serving as a **RAM** via a NOT circuit IC4. A chip enable input terminal, the inverse of CE of an IC2 serving as a mask **ROM storing** a control **program** of the IC2 is connected to an external terminal, the inverse of ROMCE. When the IC1 is actuated by the control program of the IC2, the terminal A15 is connected to the terminal, the inverse of ROMCE at the outside of a chip. While both (a) and (b) of a selection switch C1 are connected to each other when the IC1 is actuated by an IC5 serving as a mask **ROM storing** the control **programs** of IC excepting for the IC2. Thus the terminal A15 is inputted to (a), (b) and then the inverse of CE is connected to the IC5.

17/5/20 (Item 20 from file: 347)
DIALOG(R)File 347:JAPIO
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02230655 **Image available**
INTEGRATED CIRCUIT INCORPORATING PROGRAM

PUB. NO.: 62-147555 [JP 62147555 A]
PUBLISHED: July 01, 1987 (19870701)
INVENTOR(s): KANATSU JUN
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 60-289574 [JP 85289574]
FILED: December 23, 1985 (19851223)
INTL CLASS: [4] G06F-013/00
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 645, Vol. 11, No. 378, Pg. 100,
December 10, 1987 (19871210)

ABSTRACT

PURPOSE: To facilitate the change and addition of **programs** by constituting a **memory storing programs** of a **ROM** where the **program** is written and a **RAM** where the **program** can be written from the

outside.

CONSTITUTION: When an integrated circuit 1 incorporating a program is initialized, the program stored in a ROM 10 reads out a program code stored in an external memory 13 to a control circuit 12 via this circuit 12 and an external interface line 100. This program code is put on a writing data line 101 and then written on a RAM 11. The program loading operation finishes when all program codes are written. Hereafter the program stored in the RAM 11 or the ROM 10 is used to carry out the processing. In such a way, the programs can be easily changed and added.

17/5/21 (Item 21 from file: 347)
DIALOG(R)File 347:JAPIO
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00756265 **Image available**
INTEGRATED CIRCUIT

PUB. NO.: 56-076565 [JP 56076565 A]
PUBLISHED: June 24, 1981 (19810624)
INVENTOR(s): TAKAI AKIRA
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 54-153941 [JP 79153941]
FILED: November 28, 1979 (19791128)
INTL CLASS: [3] H01L-027/10; G11C-011/34; H01L-021/265
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components); 45.2
(INFORMATION PROCESSING -- Memory Units)
JAPIO KEYWORD: R100 (ELECTRONIC MATERIALS -- Ion Implantation)
JOURNAL: Section: E, Section No. 73, Vol. 05, No. 141, Pg. 101,
September 05, 1981 (19810905)

ABSTRACT

PURPOSE: To readily identify the code corresponding to the content stored in an ROM by ion implanting correspondingly to the content of the read - only memory ROM at a part of the cell of a random access memory RAM .

CONSTITUTION: An RAM2 and ROM3 are formed on a chip 1, and a matrix is formed by respective memory cells 4, 5. Address signal lines 6-9 and output lines 11-14 are connected to the RAM2, and address signal lines 16-19 and output lines 21-24 are connected to the ROM3. The hatched part in the memory cell 5 designates ion implanted part. The ions are implanted simultaneously on the load resistance element transistor 28 of the memory cell 4 of the special address (group designated by the address line 6) of the RAM2 corresponding to the ion implanted part in response to the ROM code with the ROM . This can obtained 1, 0, 1, 0 in the output lines 11-14 at the output of the RAM2. This is 5 in hexacode, and can identify that the ROM3 is manufactured in fifth order.

17/5/32 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014037347 **Image available**
WPI Acc No: 2001-521560/200157
Related WPI Acc No: 2001-281411; 2001-335399; 2001-381328; 2001-595093;
2002-337581; 2002-506744

XRPX Acc No: N01-386479

Smart card system for financial and commercial transaction, has operating system with memory manager which allocates memory space in response to command

Patent Assignee: CARPER T (CARP-I); HEMMO D (HEMM-I); CRYPTEC SYSTEMS INC (CRYP-N)

Inventor: CARPER T; HEMMO D

Number of Countries: 020 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200116759	A1	20010308	WO 2000US80	A	20000105	200157 B
US 6480935	B1	20021112	US 99116243	A	19990115	200278
			US 99386286	A	19990831	

Priority Applications (No Type Date): US 99386286 A 19990831; US 99116243 P 19990115

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
WO 200116759	A1	E	35 G06F-012/00	
Designated States (National): SG				
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE				
US 6480935	B1		G06F-012/02	Provisional application US 99116243

Abstract (Basic): WO 200116759 A1

NOVELTY - The smart card system has a microprocessor and a memory element such as random access memory (RAM), read/write memory, read only memory (ROM). The memory element stores one application and operating system (OS). The operating system has a memory manager which allocates memory space in response to a command.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

- (a) System managing smart card memory;
- (b) Method of managing smart card memory;
- (c) Method of allocating or de-allocating memory space in smart card

USE - For financial and commercial transactions.

ADVANTAGE - Provides a platform upon which a smart card is downloaded and runs several applications from different sources, without breaching data security between the applications and without inefficiently partitioning memory according to application . Since all requests for smart card memory definition are controlled by memory manager, memory integrity and security are assured. Since memory allocation is made dynamically on an as-needed basis, the smart card memory is efficiently used and need not be pre-allocated are defined by arbitrary boundaries.

DESCRIPTION OF DRAWING(S) - The figure shows the smart memory management system.

pp; 35 DwgNo 3/8

Title Terms: SMART; CARD; SYSTEM; FINANCIAL; COMMERCIAL; TRANSACTION; OPERATE; SYSTEM; MEMORY; MANAGE; ALLOCATE; MEMORY; SPACE; RESPOND; COMMAND

Derwent Class: T01; T04

International Patent Class (Main): G06F-012/00; G06F-012/02

International Patent Class (Additional): G06K-005/00; G06K-019/06; G06K-019/07

File Segment: EPI

DIALOG(R)File 350:Derwent WPIX
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012166966 **Image available**

WPI Acc No: 1998-583878/199849

Related WPI Acc No: 1999-215176; 2001-482089; 2002-689577

XRPX Acc No: N98-454834

Microcontroller integrated circuit e.g. for connecting computer system having host processor to ISDN interface - has processor and memory structure having ROM memory space to store program code in it and has dual port RAM to connect between computer and processor with dual port RAM having RAM memory space to store program code in it

Patent Assignee: KLINGMAN E E (KLIN-I)

Inventor: KLINGMAN E E

Number of Countries: 021 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9848356	A1	19981029	WO 98US8224	A	19980423	199849 B
US 5860021	A	19990112	US 97846118	A	19970424	199910

Priority Applications (No Type Date): US 97846118 A 19970424

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
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WO 9848356	A1	E 34	G06F-013/00	
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Designated States (National): CA JP US

Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU

MC NL PT SE

US 5860021	A		G06F-015/76
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Abstract (Basic): WO 9848356 A

The microcontroller integrated circuit comprises a local processor. A dual port RAM addressable by the host processor and the local processor and has a set memory space storing program code and a set second memory space stores data, so the host processor and the local processor can simultaneously access the second memory space and the host processor can further access the two memory spaces when it resets the local processor while the local processor is in reset and when the local processor is not in reset.

The local processor can access the two memory spaces. The local processor includes a reset input terminal responsive to a reset signal from the host processor to reset the local processor when the reset signal is in an active state and releases the local processor from reset when the reset signal is not in an active state. The host processor is prevented from accesses the first memory space when the reset signal is not activated.

ADVANTAGE - Provides improved microcontroller to facilitate interfacing of computer to ISDN network.

Dwg.3/7

Title Terms: INTEGRATE; CIRCUIT; CONNECT; COMPUTER; SYSTEM; HOST; PROCESSOR ; ISDN; INTERFACE; PROCESSOR; MEMORY; STRUCTURE; ROM ; MEMORY; SPACE; STORAGE; PROGRAM; CODE; DUAL; PORT; RAM ; CONNECT; COMPUTER; PROCESSOR; DUAL; PORT; RAM ; RAM ; MEMORY; SPACE; STORAGE; PROGRAM; CODE

Derwent Class: T01

International Patent Class (Main): G06F-013/00; G06F-015/76

International Patent Class (Additional): G06F-013/38

File Segment: EPI

17/5/44 (Item 23 from file: 350)
DIALOG(R)File 350:Derwent WPIX

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011699688 **Image available**

WPI Acc No: 1998-116598/199811

XRPX Acc No: N98-093510

IC card used as information memory media - has CPU that converts application program stored in RAM using language conversion program stored in ROM

Patent Assignee: DAINIPPON PRINTING CO LTD (NIPQ)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 10003526	A	19980106	JP 96153563	A	19960614	199811 B

Priority Applications (No Type Date): JP 96153563 A 19960614

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

JP 10003526 A 10 G06K-019/07

Abstract (Basic): JP 10003526 A

The IC card includes a CPU (18) and a ROM (12). The ROM stores a CPU executable general purpose program . A RAM (16) stores an executable application program according to necessity.

The ROM stores a language conversion program which is used to convert program of predetermined language to a CPU executable language. The RAM stores the application program which is converted using language conversion program.

ADVANTAGE - Enables introduction of application program with predetermined language into memory .

Dwg.1/7

Title Terms: IC; CARD; INFORMATION; MEMORY; MEDIUM; CPU; CONVERT; APPLY; PROGRAM; STORAGE; RAM ; LANGUAGE; CONVERT; PROGRAM; STORAGE; ROM

Derwent Class: T01; T04

International Patent Class (Main): G06K-019/07

International Patent Class (Additional): G06F-009/45; G06K-017/00

File Segment: EPI

17/5/62 (Item 41 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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008182062 **Image available**

WPI Acc No: 1990-069063/199010

XRPX Acc No: N90-052865

Integrated circuit card and method for writing information - comprises ROM for storing system program , EEPROM for storing application program and static RAM for storing processed data

Patent Assignee: HITACHI MAXELL KK (HITM)

Inventor: SHINAGAWA T

Number of Countries: 004 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 357361	A	19900307	EP 89308694	A	19890829	199010 B
US 5200600	A	19930406	US 89398474	A	19890825	199316
			US 92925416	A	19920810	
EP 357361	B1	19940504	EP 89308694	A	19890829	199418
DE 68915082	E	19940609	DE 615082	A	19890829	199424
			EP 89308694	A	19890829	

Priority Applications (No Type Date): JP 88214522 A 19880829
Cited Patents: 1.Jnl.Ref; A3...9044; EP 213534; EP 251619; EP 275510; FR
2591006; FR 2609175; No-SR.Pub; US 4001550; US 4211919; WO 8707062

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 357361	A	E	11		
Designated States (Regional): DE FR GB					
US 5200600	A		10	G06K-019/06	Cont of application US 89398474
EP 357361	B1	E	14	G07F-007/10	
Designated States (Regional): DE FR GB					
DE 68915082	E			G07F-007/10	Based on patent EP 357361

Abstract (Basic): EP 357361 A

The IC card (1) stores information transmitted from an external terminal unit includes a processor (3). A first memory (6) stores a system program, a second memory (4) storing an application program and third memory storing processed data to be written in second memory.

The first memory is a mask ROM whilst the third memory is a static RAM. The second memory is formed on a single chip and includes a latch circuit (4a) for temporarily latching data of a series of bytes transmitted to the IC card. An electrically erasable and programmable memory (4b) stores data of a predetermined number of bytes when data is transferred.

USE/ADVANTAGE - Method for writing information so that information processing program can be written by down-loading in non-volatile EEPROM.

1/5

Title Terms: INTEGRATE; CIRCUIT; CARD; METHOD; WRITING; INFORMATION;
COMPRISE; ROM; STORAGE; SYSTEM; PROGRAM; EEPROM; STORAGE; APPLY;
PROGRAM; STATIC; RAM; STORAGE; PROCESS; DATA
Derwent Class: T01; T04; T05
International Patent Class (Main): G06K-019/06; G07F-007/10
File Segment: EPI

17/5/63 (Item 42 from file: 350)

DIALOG(R)File 350:Derwent WPIX
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008128809 **Image available**
WPI Acc No: 1990-015810/199003
XRPX Acc No: N90-012146

Integrated circuit card for computer - has special CPU storage area to hold either test program or applications program depending on which CPU wants

Patent Assignee: MITSUBISHI DENKI KK (MITQ)
Inventor: FUJIOKA S; FURUTA S; INOUE T; MATSUBARA T; TAKAHIRA K; YAMAGUCHI
A

Number of Countries: 003 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 3844032	A	19900104	DE 3844032	A	19881227	199003 B
FR 2633756	A	19900105				199008
US 5019970	A	19910528	US 88276539	A	19881128	199124
DE 3844032	C2	19940310	DE 3844032	A	19881227	199409

Priority Applications (No Type Date): JP 88160746 A 19880630

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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DE 3844032 A 13
DE 3844032 C2 13 G06F-012/06

Abstract (Basic): DE 3844032 A

The chip board has a first control device (13,14) to form a first memory arrangement in which at least a part of a first program (3) containing a test program is superimposed on a special area in the CPU's storage zone. This special area is accessible by using a command word shorter than those used for accessing the other areas. A second control device (19,21) forms a second memory arrangement in which a part of a second **memory** containing an **applications program** is superimposed on the special area.

A detector (22) recognises whether the CPU is executing a test or applications program. Changeover devices (18,20) actuate the first control devices when the CPU is to run a test and actuate the second control devices when the CPU is to run the applications program.

ADVANTAGE - Uses special area to execute test or applications program.

1/8

Title Terms: INTEGRATE; CIRCUIT; CARD; COMPUTER; SPECIAL; CPU; STORAGE; AREA; HOLD; TEST; PROGRAM; APPLY; PROGRAM; DEPEND; CPU

Derwent Class: T01; T04

International Patent Class (Main): G06F-012/06

International Patent Class (Additional): G06F-009/00; G06K-019/00

File Segment: EPI

17/5/66 (Item 45 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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007477900 **Image available**

WPI Acc No: 1988-111834/198816

XPX Acc No: N88-084948

Smart card able to set security level for every memory area - has secret identification number area and allows access only after entered number is confirmed

Patent Assignee: TOPPAN MOORE CO LTD (TOPP)

Inventor: WATANABE H

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 4734568	A	19880329	US 86891876	A	19860730	198816 B

Priority Applications (No Type Date): JP 85169236 A 19850731

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 4734568	A	19		

Abstract (Basic): US 4734568 A

Memory areas store data in accordance with their kinds. A security level memory area stores the input condition of the secret identification number.

In a CPU (40) another CPU(401) performs the controls according to **programs** , a ROM(402) **stores** the **programs** and the like, and a **RAM** (403) temporarily **stores** data during execution of **program** steps. The **memory** chip (41) has a **PROM** in which data are mainly stored.

2/16

Title Terms: SMART; CARD; ABLE; SET; SECURE; LEVEL; MEMORY; AREA; SECRET; IDENTIFY; NUMBER; AREA; ALLOW; ACCESS; AFTER; ENTER; NUMBER

Derwent Class: T01; T04

20/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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06848440 **Image available**
ONE-CHIP MICROCOMPUTER AND SELF-WRITING SYSTEM THEREFOR

PUB. NO.: 2001-075940 [JP 2001075940 A]
PUBLISHED: March 23, 2001 (20010323)
INVENTOR(s): MORIYAMA FUMITO
APPLICANT(s): HITACHI LTD
APPL. NO.: 11-250980 [JP 99250980]
FILED: September 06, 1999 (19990906)
INTL CLASS: G06F-015/78; G06K-019/00

ABSTRACT

PROBLEM TO BE SOLVED: To make a one-chip microcomputer for IC card into Z-TAT (to supply a product requested by a user without wait) by storing a program for program write in a storage device.

SOLUTION: A one-chip microcomputer 1 for IC card has a storage device (memory) 12 composed of a RAM 12A, an E2PROM 12B and a mask ROM 12C. In the E2PROM 12B, the program for program write is stored beforehand. According to this program for program write, a program is written in the empty memory of the E2PROM 12B. The data capacity of write data from the side of personal computer and the write data are transmitted to the IC card 1. The IC card 1 successively writes received codes in its own program memories (empty memories of the E2PROM 12B).

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20/5/7 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO
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05822373 **Image available**
ELECTRONIC DEVICE

PUB. NO.: 10-105473 [JP 10105473 A]
PUBLISHED: April 24, 1998 (19980424)
INVENTOR(s): OOGIKU MAKOTO
APPLICANT(s): TOKICO LTD [000305] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-256447 [JP 96256447]
FILED: September 27, 1996 (19960927)
INTL CLASS: [6] G06F-012/14; G06K-017/00
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 45.3 (INFORMATION PROCESSING -- Input Output Units)
JAPIO KEYWORD:R005 (PIEZOELECTRIC FERROELECTRIC SUBSTANCES); R011 (LIQUID CRYSTALS); R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessors)

ABSTRACT

PROBLEM TO BE SOLVED: To prevent information stored in a memory from being leaked to an outside.

SOLUTION: The control circuit 6 of an IC card device 1 starts the interruption processing of an erasion program when a detection switch 36 is turned on, permits maintenance work when the input of a maintenance password code from a password code input switch 29 is recognized and erases

a control program and data stored in EEPROM 9 at the time of no maintenance password code input. Therefore, unless the maintenance password code is inputted even when the detection switch 36 is turned on or when the inputted maintenance password code is wrong, it is surely prevented that maintenance 33 is opened and the control program and data stored in SRAM 8 are robbed in order to erase the control program and respective kinds of data stored in SRAM 8.

20/5/21 (Item 21 from file: 347)
DIALOG(R)File 347:JAPIO
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03792436 **Image available**
ELECTRONIC COMPUTER DEVICE

PUB. NO.: 04-157536 [JP 4157536 A]
PUBLISHED: May 29, 1992 (19920529)
INVENTOR(s): KIHARA HIROTAKA
MIZUNAGA CHIHU
APPLICANT(s): SHARP CORP [000504] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 02-283694 [JP 90283694]
FILED: October 22, 1990 (19901022)
INTL CLASS: [5] G06F-011/22
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JAPIO KEYWORD: R139 (INFORMATION PROCESSING -- Word Processors)
JOURNAL: Section: P, Section No. 1423, Vol. 16, No. 448, Pg. 141,
September 17, 1992 (19920917)

ABSTRACT

PURPOSE: To speed up test program actuation and to facilitate test program update by storing a test program in a semiconductor memory which can be connected to a main memory.

CONSTITUTION: An IC card 21 includes a memory 23 composed of a ROM or RAM and the memory 23 is connected to the address bus and data bus of the device main body through an IC card interface 20 and receives a source voltage and a chip select signal. Then an instruction for indicating the start of the test program is inputted and when it is decided that the IC card 21 stored with the test program is inserted into the main body, the control of a test program CPU 22 stored on the IC card 21 is transferred and the test program is started. Consequently, the test program is started at a high speed and easily updated.

20/5/25 (Item 25 from file: 347)
DIALOG(R)File 347:JAPIO
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03619703 **Image available**
ROM CARD WRITING SYSTEM FOR CONTROL PROGRAM

PUB. NO.: 03-282603 [JP 3282603 A]
PUBLISHED: December 12, 1991 (19911212)
INVENTOR(s): YOSHIDA KAZUO
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-082837 [JP 9082837]
FILED: March 29, 1990 (19900329)

INTL CLASS: [5] G05B-019/18
JAPIO CLASS: 22.3 (MACHINERY -- Control & Regulation)
JAPIO KEYWORD: R063 (MACHINERY -- Numerical Control Machine Tools, NC)
JOURNAL: Section: P, Section No. 1326, Vol. 16, No. 109, Pg. 76, March
17, 1992 (19920317)

ABSTRACT

PURPOSE: To effectively use the memory capacity by unloading a **RAM** card out of a numerical controller after **storing** a **program** into the card, loading the **RAM** card into a **ROM** cut-off device together with a **ROM** card, and copying the contents of the **RAM** card on the **ROM** card.

CONSTITUTION: A **program** is **stored** in a **RAM** card 4 containing a back-up means for holding the storage data. Then the card 4 is taken out of a numerical controller 1 and loaded into a **ROM** cut-off device 12 set separately together with a **ROM** card 11. The device 12 copies the **program** **stored** in the **card** 4 on the card 11. Thus it is just required to newly provide a **RAM** card from which the **ROM** cut-off function is eliminated despite the increase of the capacity of a **software memory** so as to **obtain** a **ROM** writing system for control **program** that is not required to **store** the **ROM** cut-off function **software** into a **RAM** area.

20/5/26 (Item 26 from file: 347)
DIALOG(R)File 347:JAPIO
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03610478 **Image available**
NON-CONTACT TYPE PORTABLE STORING MEDIUM PROCESSING SYSTEM

PUB. NO.: 03-273378 [JP 3273378 A]
PUBLISHED: December 04, 1991 (19911204)
INVENTOR(s): HINOTO OKIFUMI
APPLICANT(s): OMRON CORP [000294] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 02-075275 [JP 9075275]
FILED: March 22, 1990 (19900322)
INTL CLASS: [5] G07B-011/00
JAPIO CLASS: 29.4 (PRECISION INSTRUMENTS -- Business Machines)
JAPIO KEYWORD: R073 (TRANSPORTATION -- Automatic Wickets); R131 (INFORMATION
PROCESSING -- Microcomputers & Microprocessors)
JOURNAL: Section: P, Section No. 1321, Vol. 16, No. 92, Pg. 116, March
06, 1992 (19920306)

ABSTRACT

PURPOSE: To simplify a ticket examination processing or the like by executing a command at a storing medium when an identification code to be transmitted together with the command from a main unit is coincident with a previously stored identification code in a processing system to exchange data with the main unit.

CONSTITUTION: When an **IC card** 2 of the portable storing medium is inserted to the enable range of communication with the main unit 1 connected to an antenna 8 while providing a CPU 3, **ROM** 4 for **storing** a **program** or the like, **RAM** 3, I/F 6 and read/write controller 7 or the like, the command and card identification information from the unit 1 are received at the card 2 and compared with the identification number of the card 2 read out from an **EEPROM** 12 or the like. When they are coincident, the command from the unit 1 is executed. Thus, the ticket examination processing or the like is easily executed without taking out a season

ticket or the like from the case.

20/5/30 (Item 30 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2003 JPO & JAPIO. All rts. reserv.

03304715 **Image available**
MICROCOMPUTER

PUB. NO.: 02-280215 [JP 2280215 A]
PUBLISHED: November 16, 1990 (19901116)
INVENTOR(s): KIMURA TAKASHI
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation)
, JP (Japan)
APPL. NO.: 01-102276 [JP 89102276]
FILED: April 21, 1989 (19890421)
INTL CLASS: [5] G06F-001/26; G06F-015/78
JAPIO CLASS: 45.9 (INFORMATION PROCESSING -- Other); 45.4 (INFORMATION
PROCESSING -- Computer Applications)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers &
Microprocessors)
JOURNAL: Section: P, Section No. 1162, Vol. 15, No. 47, Pg. 31,
February 05, 1991 (19910205)

ABSTRACT

PURPOSE: To reduce a microcomputer consumption current and, simultaneously, to stabilize an operation by operating a **program storage** means, a **program** address designating means, a data **storage** means, a logic arithmetic circuit and an oscillation circuit in making a voltage outputted from a constant voltage circuit into a power source.

CONSTITUTION: By a constant voltage circuit 16 from the power voltage, the constant voltage lower than the power voltage is generated, the outputted voltage is made into the power source, and a **ROM** 11, a **RAM** 12, a **program** counter 13, an ALU 14 and an oscillation circuit 15 to compose the microcomputer are driven. Thus, the most part of an **integrated circuit** to compose the microcomputer can be driven in making the voltage lower than the power voltage into the power source, and the consumption current can be widely reduced in comparison with the case of the microcomputer to be directly driven with the power voltage to be conventional. In the case of using a battery for the power source, the malfunction of the microcomputer due to the fluctuation of the battery voltage can be suppressed.

20/5/34 (Item 34 from file: 347)
DIALOG(R)File 347:JAPIO
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02780711 **Image available**
INFORMATION PROCESSOR

PUB. NO.: 01-078311 [JP 1078311 A]
PUBLISHED: March 23, 1989 (19890323)
INVENTOR(s): KITATSUME YOSHIAKI
KOYAMA TAKUO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 62-234808 [JP 87234808]
FILED: September 21, 1987 (19870921)

INTL CLASS: [4] G06F-001/00
JAPIO CLASS: 45.9 (INFORMATION PROCESSING -- Other)
JAPIO KEYWORD: R129 (ELECTRONIC MATERIALS -- Super High Density **Integrated Circuits**, LSI & GS; R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessors
JOURNAL: Section: P, Section No. 896, Vol. 13, No. 303, Pg. 98, July 12, 1989 (19890712)

ABSTRACT

PURPOSE: To realize application of many types of application software just with a single unit of information processor by putting a processing part which consists of an **IC card** or a print board module into a housing containing a keyboard, a display part, an external memory, etc.

CONSTITUTION: The size of a processing part 10 is reduced by means of a highly **integrated circuit** as a sheet of **IC card** or a compact print board module. Then such a part 10 is properly added to an information processor in response to the desired application software. In this case, the application software corresponding to a microprocessor 1 integrated to the part 10 is stored into a **ROM** 2 included in the part 10. Otherwise a means is added to the part 10 to identify the device type of the microprocessor 1. Then the applicable **application** softwares are **listed** up at the system initialization. Thus it is urged to load the **application software** into a built-in **RAM** 3 from an external memory. As a result, various types of application software are available just with a single unit of information processor.

20/5/35 (Item 35 from file: 347)
DIALOG(R) File 347:JAPIO
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02756933 **Image available**
PROCESSOR

PUB. NO.: 01-054533 [JP 1054533 A]
PUBLISHED: March 02, 1989 (19890302)
INVENTOR(s): IDE DAISAKU
APPLICANT(s): NEC ENG LTD [329822] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-211696 [JP 87211696]
FILED: August 26, 1987 (19870826)
INTL CLASS: [4] G06F-009/22; G06F-009/06
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JAPIO KEYWORD: R129 (ELECTRONIC MATERIALS -- Super High Density **Integrated Circuits**, LSI & GS; R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessors
JOURNAL: Section: P, Section No. 885, Vol. 13, No. 261, Pg. 28, June 16, 1989 (19890616)

ABSTRACT

PURPOSE: To decrease the number of times of the manufacture of a technical sample, and to remarkably shorten the development period, by switching and outputting a substitute **program** stored in a **RAM** so as to correspond to a program and an address, in accordance with an instruction at the time of access to a **ROM**.

CONSTITUTION: When a part to be corrected has been generated in a microprogram stored in a **ROM** 5, in an address of a **RAM** 6 corresponding to its part, an address of a **RAM** 7 in which a corrected micro-instruction

has been stored in written, and when an address of its part has been designated by an access to the ROM 5, the corrected micro-instruction outputted from the RAM 7 is selected by a selector 9 in accordance with an output signal 103 of the RAM 6 and sent out to an instruction unit 1. In such a way, a partial correction of the program of the ROM 5 can be executed. Also, by storing a branch instruction in the RAM 7, and storing the corrected micro-instruction in a RAM 8, a correction of only a word number portion of the RAM 7 can be executed. By the constitution which considers the capacity balance of said RAM 7 and 8, the performance deterioration is reduced and the correction quantity can be enlarged.

20/5/37 (Item 37 from file: 347)
DIALOG(R)File 347:JAPIO
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02491559 **Image available**
DATA PROCESSOR

PUB. NO.: 63-108459 [JP 63108459 A]
PUBLISHED: May 13, 1988 (19880513)
INVENTOR(s): IGASAKI TOSHIAKI
APPLICANT(s): TOKYO ELECTRIC CO LTD [000356] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-255167 [JP 86255167]
FILED: October 27, 1986 (19861027)
INTL CLASS: [4] G06F-015/24; G06F-013/00
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 762, Vol. 12, No. 359, Pg. 18, September 27, 1988 (19880927)

ABSTRACT

PURPOSE: To enable addition and correction of a **program** only by changing a **memory** card in a method whereby various work **programs** are stored in a **ROM** and a **RAM**, as well as in the memory card, and selectively read out for executing the work.

CONSTITUTION: A CPU 11 executes the picture display processing based on basic **program** data stored into a **ROM** 12. First, it is investigated whether or not a memory card 6 is loaded, and if load, investigation is continued whether or not the **program** data are stored in the card 6. When the data are stored, for the **program** of the card 6, a selecting number and a program name are displayed by adding selecting symbols A and I to a liquid crystal display 3. Next, it is investigated whether or not the **program** data are stored in a **RAM** 13, and when the data are stored, they are displayed at the display 3. For the displaying, selecting symbols U, E, O and K are added, the **program** of the **RAM** 13 composed of the selecting number and the program name is displayed, and when the program is absent, nothing is displayed.

20/5/42 (Item 42 from file: 347)
DIALOG(R)File 347:JAPIO
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01526816 **Image available**
INFORMATION RETRIEVING DEVICE

PUB. NO.: 60-005316 [JP 60005316 A]

PUBLISHED: January 11, 1985 (19850111)
INVENTOR(s): NISHIMURO YOSHIAKI
APPLICANT(s): CANON INC [000100] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 58-111804 [JP 83111804]
FILED: June 23, 1983 (19830623)
INTL CLASS: [4] G06F-003/02; G06F-007/28
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 45.1
(INFORMATION PROCESSING -- Arithmetic Sequence Units); 45.2
(INFORMATION PROCESSING -- Memory Units)
JAPIO KEYWORD: R106 (INFORMATION PROCESSING -- Kanji Information Processing)
; R129 (ELECTRONIC MATERIALS -- Super High Density
Integrated Circuits, LSI & GS; R131 (INFORMATION
PROCESSING -- Microcomputers & Microprocessors
JOURNAL: Section: P, Section No. 358, Vol. 09, No. 120, Pg. 58, May
24, 1985 (19850524)

ABSTRACT

PURPOSE: To improve the efficiency of the converting operation of a Kana (Japanese syllabary)-to-Kanji (Chinese character) converter, by informing at first to the operator about the matter when information corresponding to the information inputted into the converter is not stored in a fixed memory.

CONSTITUTION: A Kana input key group K1, Kanji conversion key K2, and fixed memory M1 are connected to a CPU and, in addition to the above, a display DIS is also connected to the CPU through a display driver DR. The CPU is constituted of, for example, an 1-chip SLI; and a control section, **ROM** which stores programs, **RAM**, Kana input key depressing frequency counter N, etc., are installed to the inside of the CPU. Whenever input operation is performed while the way of reading of a Kanji is inputted through the Kana key group K1, it is retrieved that whether or not the way of reading is the same as that already inputted and Kanji information starting by the way of reading which is already inputted and ended is stored in a memory M1 or not and, when the Kanji information is not stored, the last inputted way of reading is informed to the operator by means of flashing display.

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25/5/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010742180 **Image available**
WPI Acc No: 1996-239135/199624
XRPX Acc No: N96-200206

File management system for non- volatile IC card - performs data management of files using directory for managing files divided into field length fields, each contg. file definition and assigns data for specifying file definition to each field

Patent Assignee: TOSHIBA KK (TOKE)

Inventor: IIJIMA Y

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5515532	A	19960507	US 94309598	A	19940921	199624 B

Priority Applications (No Type Date): JP 93259267 A 19930922

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 5515532	A	21	G06F-013/00	

Abstract (Basic): US 5515532 A

The directory information including fixed data which remains unchanged despite any change in the files and variable data which is dependent on a change in the **files** is **stored**. The fixed data contains **file** identification information, file size information, and first check information for checking validity of the fixed data. The variable data contains unused file size information indicating unused size of any of the **files** in the **memory**, and second check information for checking validity of the variable data. The **directory** information of a target **file** which is to be **accessed** is **searched**, based on the **file** identification information.

A first verify system is provided for verifying the validity of the fixed data included in the searched directory information, based on the first check information contained in the fixed data. A second verify system is provided for verifying the validity of the variable data included in the searched directory information, based on the second check information contained in the variable data. Target file is erased when the first verify system verifies the validity of the fixed data. The target **file** is **accessed** when the first verify system verifies the validity of the fixed data and the second verify system verifies the validity of the variable data.

USE/ADVANTAGE - File management system for managing **files** in **memory**, based on directory information defining **files** in **memory**. Allows **access** to other definition information in card, even if card directory is locally damaged or destroyed, e.g. by illegal removal of card. Assures authenticity of fixed data even when variable data is destroyed.

Dwg.2/17

Title Terms: FILE; MANAGEMENT; SYSTEM; NON; **VOLATILE** ; IC; CARD;
PERFORMANCE; DATA; MANAGEMENT; FILE; DIRECTORY; MANAGE; FILE; DIVIDE;
FIELD; LENGTH; FIELD; CONTAIN; FILE; DEFINE; ASSIGN; DATA; SPECIFIED;
FILE; DEFINE; FIELD

Derwent Class: T01

International Patent Class (Main): G06F-013/00

International Patent Class (Additional): G06F-017/30

File Segment: EPI

27/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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06471711 **Image available**

IC CARD INCORPORATED WITH PLURAL REWRITABLE NONVOLATILE MEMORIES

PUB. NO.: 2000-057286 [JP 2000057286 A]
PUBLISHED: February 25, 2000 (20000225)
INVENTOR(s): YAMADA MASANARI
SAITO HIROO
IRISAWA KAZUYOSHI
MORIYAMA AKIKO
SHIBATA NAOTO
APPLICANT(s): DAINIPPON PRINTING CO LTD
APPL. NO.: 10-224431 [JP 98224431]
FILED: August 07, 1998 (19980807)
INTL CLASS: G06K-019/07; G06K-019/073

ABSTRACT

PROBLEM TO BE SOLVED: To surely perform data protection for a user and to improve the reliability of an IC card by incorporating a nonvolatile memory for system area and a nonvolatile memory for user area into the IC card.

SOLUTION: This IC card 2 has a CPU 2a, a RAM 2b, a ROM 2c, a nonvolatile memory M1 for a system area and a nonvolatile memory M2 for a user area. When a program stored in the ROM 2c is read to the CPU 2a and a command transmitted from a reader/writer is received, data transmitted together with the command is read, needed processing is performed and results are written in the memories M1 and M2. Also, a flag during writing is set in the system area, when writing is performed in the user area, the flag is made 1 just before the writing, and when the writing is normally finished, the flag is made 0.

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27/5/4 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO
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06131837 **Image available**

IC CARD

PUB. NO.: 11-073375 [JP 11073375 A]
PUBLISHED: March 16, 1999 (19990316)
INVENTOR(s): HAYASHI MASAHIRO
IRISAWA KAZUYOSHI
APPLICANT(s): DAINIPPON PRINTING CO LTD
APPL. NO.: 09-233942 [JP 97233942]
FILED: August 29, 1997 (19970829)
INTL CLASS: G06F-012/14; G06K-017/00; G06K-019/073

ABSTRACT

PROBLEM TO BE SOLVED: To make it possible to internally execute ciphering processing by an IC card by making it possible to specify a storing position of a disclosed key from the outside without requiring a key file for the disclosed key.

SOLUTION: In an IC card having a CPU, a RAM an EEPROM (electrically

erasable programmable read - only memory), and an ROM and loading a coprocessor, the EEPROM has a data file for storing one or more RSA disclosed cipher keys allowed to be read out by respective identifiers(IDs) and a key file for storing one or more RSA secret keys. A certain disclosed cipher key is specified by an ID based on an instruction from the external, a secret key is specified by an exclusive command and the coprocessor executes data ciphering/deciphering processing by using the disclosed cipher key and the secret key.

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27/5/5 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO
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05957791 **Image available**
IC CARD

PUB. NO.: 10-240891 [JP 10240891 A]
PUBLISHED: September 11, 1998 (19980911)
INVENTOR(s): KOBAYASHI TOYOAKI
APPLICANT(s): OKI ELECTRIC IND CO LTD [000029] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-038698 [JP 9738698]
FILED: February 24, 1997 (19970224)
INTL CLASS: [6] G06K-019/073; G06F-012/14
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 30.1 (MISCELLANEOUS GOODS -- Office Supplies); 45.2 (INFORMATION PROCESSING -- Memory Units)
JAPIO KEYWORD:R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessors); R303

ABSTRACT

PROBLEM TO BE SOLVED: To prevent the IC card with extended function from being illegally executed.

SOLUTION: This IC card 1 is provided with a storage area for housing a program and EEPROM 5 housing a registering condition information, which is set respectively corresponding to a storing area and housed in RAM 4 as password collating information when a password is released at the time of housing a program to specify the storage area housing the program based on the command when an area selection command is inputted and to select registering condition information corresponding to the specified area. Then, a command code and executing condition information for recognizing whether the program can be executed by the command are inputted, the selected registering condition information and a password collating information housed in RAM 4 are compared with each other. When these information are matched with each other, the command code, executing condition information and the leading address of a specified storing area are respectively registered in EEPROM 5.

27/5/9 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO
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05705048 **Image available**
PORTABLE DATA CARRIER

PUB. NO.: 09-319848 [JP 9319848 A]

PUBLISHED: December 12, 1997 (19971212)
INVENTOR(s): YURA AKIYUKI
TAKAYAMA FUMIHIRO
HIRANO SEIJI
APPLICANT(s): TOPPAN PRINTING CO LTD [000319] (A Japanese Company or
Corporation), JP (Japan)
APPL. NO.: 08-135058 [JP 96135058]
FILED: May 29, 1996 (19960529)
INTL CLASS: [6] G06K-019/073; G06K-017/00
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 30.1
(MISCELLANEOUS GOODS -- Office Supplies)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a portable data carrier whose issuance processing is simplified, without increasing the program capacity.

SOLUTION: When a signal RST is supplied from the outside to initialize an IC card before a series of operations, a CPU 1 which executes a program stored in a ROM 2 sets all flags on a RAM 3 to 'collated state' and retrieves each reference key from an EEPROM 4. At the time of this retrieval, the flag corresponding to a found reference key is changed to 'uncollated state'. In issuance processing which follows, a route directory is generated in the final access condition, and an MF(master file) is generated, and plural reference key files, including individual reference key data, are successively generated. Since the final access condition is set to the MF, it is unnecessary to rewrite the pertinent access condition.

27/5/10 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO
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05683031 **Image available**
PORTABLE DATA CARRIER

PUB. NO.: 09-297831 [JP 9297831 A]
PUBLISHED: November 18, 1997 (19971118)
INVENTOR(s): MATSUMURA SHUICHI
YURA AKIYUKI
YAMAOKA KENICHI
APPLICANT(s): TOPPAN PRINTING CO LTD [000319] (A Japanese Company or
Corporation), JP (Japan)
APPL. NO.: 08-112770 [JP 96112770]
FILED: May 07, 1996 (19960507)
INTL CLASS: [6] G06K-019/07; G06F-011/22; G06F-012/16
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 45.1
(INFORMATION PROCESSING -- Arithmetic Sequence Units); 45.2
(INFORMATION PROCESSING -- Memory Units)

ABSTRACT

PROBLEM TO BE SOLVED: To shorten the transmission time of commands and response of a self-diagnostic process and omit a command transmitting function of the self-diagnostic process from external equipment as to the portable data carrier (IC card).

SOLUTION: A CPU 1 which executes a program stored in a ROM 2 performs a self-diagnostic process for a RAM 3 when supplied from an RST signal from outside, and stores error information showing abnormality in a 1st specific area of the RAM 3 when detecting the abnormality. Further, the

state of an **EEPROM** area is checked and when the **IC card** is unissued, a self-diagnostic process for an **EEPROM** area is performed and information showing the diagnostic result is stored in a 2nd specific area of the **RAM** 3. Then the information stored in the 2nd specific area of the **RAM** 3 and the information stored in the 1st specific area are added to initial response data and then the initial response data are outputted.

27/5/11 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO
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05644435 **Image available**
PORTABLE INFORMATION STORAGE MEDIUM, APPLICANT INFORMATION INPUT DEVICE,
PORTABLE INFORMATION STORAGE MEDIUM SYSTEM, AND DATA ACCESS METHOD FOR
PORTABLE INFORMATION STORAGE MEDIUM

PUB. NO.: 09-259235 [JP 9259235 A]
PUBLISHED: October 03, 1997 (19971003)
INVENTOR(s): IRISAWA KAZUYOSHI
APPLICANT(s): DAINIPPON PRINTING CO LTD [000289] (A Japanese Company or
Corporation), JP (Japan)
APPL. NO.: 08-062985 [JP 9662985]
FILED: March 19, 1996 (19960319)
INTL CLASS: [6] G06K-017/00; G06F-017/60; G06K-019/073
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 45.4
(INFORMATION PROCESSING -- Computer Applications)
JAPIO KEYWORD:R011 (LIQUID CRYSTALS)

ABSTRACT

PROBLEM TO BE SOLVED: To make it possible to omit password input and prevent a password from being stolen by performing collation by a data managing means by using applicant information stored in an applicant information storage area of a nonvolatile storage means.

SOLUTION: A CPU 12 controls an **IC card** 10 according to a program in a **ROM** 13. An **EEPROM** 15, on the other hand, stores original data recorded on the **IC card** 10. A directory file in this **EEPROM** 15 is provided with an unlocking information area storing unlocking information regarding a handling person's key. Consequently, even when the **IC card** 10 is not connected to a transaction terminal device 20, etc., and can not be supplied with electric power, its unlocking information is held. The unlocking information held in the unlocking information area is copied to a **RAM** 14 before a transaction starts once the **IC card** 10 is connected to the transaction terminal device 20, and used for matching against access conditions in a subsequent transaction process.

27/5/12 (Item 12 from file: 347)
DIALOG(R)File 347:JAPIO
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05420219 **Image available**
PORTABLE INFORMATION RECORDING MEDIUM AND ITS ACCESS METHOD

PUB. NO.: 09-035019 [JP 9035019 A]
PUBLISHED: February 07, 1997 (19970207)
INVENTOR(s): IRISAWA KAZUYOSHI
APPLICANT(s): DAINIPPON PRINTING CO LTD [000289] (A Japanese Company or
Corporation), JP (Japan)

APPL. NO.: 07-202854 [JP 95202854]
FILED: July 17, 1995 (19950717)
INTL CLASS: [6] G06K-017/00
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units)

ABSTRACT

PROBLEM TO BE SOLVED: To efficiently perform external access to an IC card while guaranteeing sufficient security.

SOLUTION: A batch file formed by enumerating a plurality of commands to be executed by a CPU 12 is prepared and written in an EEPROM 15 on an IC card by using a write command. Then a specific batch process execution command is supplied successively. In a ROM 13, a routine is added which executes the respective commands in a batch file stored in the EEPROM 15 as if they were supplied from an I/O line when the command is supplied. The CPU 12 executes the commands in the batch file in order according to the routine and stores individual responses in a RAM 14 temporarily. After all the commands are executed, the stored responses are sent back together to a reader writer device 20.

27/5/13 (Item 13 from file: 347)
DIALOG(R) File 347:JAPIO
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05191940 **Image available**
IC CARD

PUB. NO.: 08-147440 [JP 8147440 A]
PUBLISHED: June 07, 1996 (19960607)
INVENTOR(s): WAKAMATSU MASAKI
HARIMA HIROTSUGU
APPLICANT(s): DAINIPPON PRINTING CO LTD [000289] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-305689 [JP 94305689]
FILED: November 16, 1994 (19941116)
INTL CLASS: [6] G06K-019/07; G06F-003/08; G06K-017/00
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 30.1 (MISCELLANEOUS GOODS -- Office Supplies)
JAPIO KEYWORD:R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessors)

ABSTRACT

PURPOSE: To detect which process interrupts the loading of an application and to disable an IC card which becomes abnormal to be reloaded.
CONSTITUTION: This IC card 100 which is equipped with at least three kinds of memory, i.e., a ROM 102, a RAM 103, and an EEPROM 104 and loads the application program in the EEPROM 104 and executes it has an application loading means which loads the application, an application executing means which executes the application program, and respective process processing and storage means which store whether respective processes of the application loading end or not; and the information stored in the respective process processing and storage means is outputted and the processing is ended when the IC card is activated again unless the information which is obtained at the time of initial application loading and stored in the respective process storage means show that all the processes end normally.

27/5/14 (Item 14 from file: 347)

DIALOG(R)File 347:JAPIO
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04979332 **Image available**
INFORMATION PROCESSOR

PUB. NO.: 07-271932 [JP 7271932 A]
PUBLISHED: October 20, 1995 (19951020)
INVENTOR(s): KITATSUME YOSHIAKI
 KOYAMA TAKUO
 HATANO TOMIHISA
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
 (Japan)
APPL. NO.: 07-004632 [JP 954632]
FILED: January 17, 1995 (19950117)
INTL CLASS: [6] G06K-017/00; G06F-003/06; G06F-003/08
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers &
 Microprocessors); R139 (INFORMATION PROCESSING -- Word
 Processors)

ABSTRACT

PURPOSE: To shorten the program loading time of application software and to fast read the data out of an external **storage** with no remodeling of the **application** software by performing the reading/writing operations of information in a single processing cycle of an arithmetic processor to a card type external storage.

CONSTITUTION: The application **software** are read out of a **ROM** 11, a **RAM** 12, etc., by an MPU 10 and undergo the prescribed processing. The result of this processing is shown on a CRT 16 via a display control circuit 15. Then a DMAC 13 is used for the DMAC transfer that is carried out between a memory and an external storage and also between the memories. An **IC card** 14 is inserted into the main body of an information processor and the contents of the card 14 are read out. These read data are sent to the **RAM** 12 of the main body of the information processor. Thus the program/data loading time can be shortened with no remodeling of the application software, and the handling facility of an information processor is improved for its users.

27/5/15 (Item 15 from file: 347)
DIALOG(R)File 347:JAPIO
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04979331 **Image available**
INFORMATION PROCESSOR

PUB. NO.: 07-271931 [JP 7271931 A]
PUBLISHED: October 20, 1995 (19951020)
INVENTOR(s): KITATSUME YOSHIAKI
 KOYAMA TAKUO
 HATANO TOMIHISA
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
 (Japan)
APPL. NO.: 07-004631 [JP 954631]
FILED: January 17, 1995 (19950117)
INTL CLASS: [6] G06K-017/00; G06F-003/06; G06F-003/08; G06F-009/445
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 45.1
 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers &

Microprocessors); R139 (INFORMATION PROCESSING -- Word Processors)

ABSTRACT

PURPOSE: To shorten the program loading time of application software and to fast read the data out of an external **storage** with no remodeling of the **application** software by using a card type external storage as either or a main storage and an external storage.

CONSTITUTION: The application **software** are read out of a **ROM** 11, a **RAM** 12, etc., by an MPU 10 and undergo the prescribed processing. The result of this processing is shown on a CRT 16 via a display control circuit 15. An **IC card** 14 is inserted into the main body of an information processor such as a personal computer, etc. Then the contents of the card 14 are read out by a power-on operation or the operation of a keyboard, and these read data are sent to the **RAM** 12 of the main body of the information processor.

27/5/18 (Item 18 from file: 347)
DIALOG(R)File 347:JAPIO
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04821897 **Image available**
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUB. NO.: 07-114497 [JP 7114497 A]
PUBLISHED: May 02, 1995 (19950502)
INVENTOR(s): AKAO YASUSHI
KURODA KENICHI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 05-282007 [JP 93282007]
FILED: October 14, 1993 (19931014)
INTL CLASS: [6] G06F-012/06; G06F-015/78
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 45.4
(INFORMATION PROCESSING -- Computer Applications)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers &
Microprocessors)

ABSTRACT

PURPOSE: To improve operability while improving productivity by loading a **nonvolatile memory** circuit on a microcomputer of one chip, a part where the processing **program** of data is **stored** as the one dedicated for readout, and using another part as the one for read/write of the data.

CONSTITUTION: The microcomputer of one chip is constituted of a microprocessor CPU and one memory FRAM using a ferroelectric capacitor, and a part of the FRAM is used as a **ROM** part in which a **program** is **stored**, and residual parts as a **RAM**. The boundary of the **ROM** part and the **RAM** part can be designated by a user arbitrarily. In this way, since the allocation of memory capacity between the **ROM** and the **RAM** is not required to consider, high productivity can be obtained in design and manufacturing, and also, the operability can be improved since a **program** **storing** area can be set arbitrarily when this device is used.

27/5/26 (Item 26 from file: 347)
DIALOG(R)File 347:JAPIO
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03705990 **Image available**

IC MEMORY CARD

PUB. NO.: 04-071090 [JP 4071090 A]
PUBLISHED: March 05, 1992 (19920305)
INVENTOR(s): INOSE SHUICHI
APPLICANT(s): CANON INC [000100] (A Japanese Company or Corporation), JP
 (Japan)
APPL. NO.: 02-182704 [JP 90182704]
FILED: July 12, 1990 (19900712)
INTL CLASS: [5] G06K-019/073; G06F-012/14; G11C-005/00
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 30.1
 (MISCELLANEOUS GOODS -- Office Supplies); 45.2 (INFORMATION
 PROCESSING -- Memory Units)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers &
 Microprocessors)
JOURNAL: Section: P, Section No. 1374, Vol. 16, No. 276, Pg. 96, June
 19, 1992 (19920619)

ABSTRACT

PURPOSE: To reduce the load of a host equipment by providing an IC memory card to be attachably/detachably loaded to the host equipment with an identification(ID) means for controlling an access to a memory and a control means and executing ID processing by the card side.

CONSTITUTION: The IC memory card 7 is provided with connectors C4 to C6, buses A, D, C, a ROM 11, a RAM 13, a control circuit 12, and the like. The RAM 13 executes the original storage function of the memory card 7. The memory card 7 is attachably/detachably connected to a bus 8 through an adaptor 6 and a CPU accesses the memory card 7 when necessary. The ROM 11 stores a control program for controlling an access to the RAM 13 based on the ID number of a user himself and the decided result of ID number check. When the memory card 7 is connected to the adaptor 6, the CPU reads out the ID number and an ID number checking control program from the ROM 11 and executes the read program .

27/5/27 (Item 27 from file: 347)

DIALOG(R)File 347:JAPIO

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03589883 **Image available**

DATA PROCESSOR

PUB. NO.: 03-252783 [JP 3252783 A]
PUBLISHED: November 12, 1991 (19911112)
INVENTOR(s): YAMAZAKI TAKANAGA
 BABA SHIRO
 KURAKAZU KEIICHI
 ANDO MASAHARU
 TANAKA NORIO
 KANEKO SUSUMU
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
 (Japan)
APPL. NO.: 02-049353 [JP 9049353]
FILED: March 02, 1990 (19900302)
INTL CLASS: [5] G06F-015/72; G09G-005/00; G09G-005/20; G09G-005/24;
 G09G-005/36
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 29.4

(PRECISION INSTRUMENTS -- Business Machines); 44.9
(COMMUNICATION -- Other)
JAPIO KEYWORD: R002 (LASERS); R011 (LIQUID CRYSTALS); R116 (ELECTRONIC
MATERIALS -- Light Emitting Diodes, LED); R129 (ELECTRONIC
MATERIALS -- Super High Density **Integrated Circuits**, LSI
& GS; R131 (INFORMATION PROCESSING -- Microcomputers &
Microprocessors
JOURNAL: Section: P, Section No. 1309, Vol. 16, No. 53, Pg. 89,
February 10, 1992 (19920210)

ABSTRACT

PURPOSE: To execute a large quantity of computation at high speed by providing a microprocessor, and a digital signal processor including a sequence control part, an execution part, and control storage on which data processing algorithm is described at one semiconductor substrate.

CONSTITUTION: A single chip microcomputer 1 comprises integrating a CPU(sub 2) as the microprocessor, the digital signal processor (DSP) 3 having a floating point computing function to perform outline font development, a direct memory access controller(DMAC) 6 having a data block transfer function such as bit block transfer, a dual port **RAM** 4, and a peripheral circuit 7 including a **ROM** which **stores** the operating **program** of the CPU(sub 2) and a serial communication interface controller(SCI) which performs data communication between the outside, etc., on one semiconductor substrate. Thereby, it is possible to execute a large quantity of computation at high speed.

27/5/29 (Item 29 from file: 347)
DIALOG(R)File 347:JAPIO
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03399500 **Image available**
INTEGRATED CIRCUIT DEVICE

PUB. NO.: 03-062400 [JP 3062400 A]
PUBLISHED: March 18, 1991 (19910318)
INVENTOR(s): ISHITSUKI NORIYOSHI
APPLICANT(s): SHARP CORP [000504] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 01-197265 [JP 89197265]
FILED: July 29, 1989 (19890729)
INTL CLASS: [5] G11C-029/00
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 42.2
(ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers &
Microprocessors)
JOURNAL: Section: P, Section No. 1211, Vol. 15, No. 220, Pg. 72, June
05, 1991 (19910605)

ABSTRACT

PURPOSE: To simplify the constitution required for the check and to reduce the required time by integrating a 2nd **storage** means **storing** a required test **program** to one and same IC for the check of a 1st storage means formed in the IC.

CONSTITUTION: When a test mode setting signal Sa is inputted from a check device via a test terminal 4a, a test mode circuit 3b outputs a test mode signal Sb and is inputted respectively to a check **ROM** 3a, a discrimination circuit 3c, and an output circuit 3d. Thus, the check

program stored in the ROM 3a is read. Then a setting data outputted from the discrimination circuit 3c is transferred to an arithmetic section 2a and fetched by the discrimination circuit 3c. When a control section 2b designates a write address to a RAM 2d, a data is written the address and then read out. Then the result of discrimination relating to the propriety of the RAM 2d is outputted from the circuit 3c to an output port 4c.

27/5/31 (Item 31 from file: 347)
DIALOG(R)File 347:JAPIO
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03379397 **Image available**
IC CARD WITH KEYBOARD DISPLAY

PUB. NO.: 03-042297 [JP 3042297 A]
PUBLISHED: February 22, 1991 (19910222)
INVENTOR(s): MASUDA HIDEKI
SHINOHARA YOSHITSUGU
HAGIWARA ISAMU
APPLICANT(s): OMRON CORP [000294] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 01-178643 [JP 89178643]
FILED: July 10, 1989 (19890710)
INTL CLASS: [5] B42D-015/10; G06F-003/033; G06K-019/07
JAPIO CLASS: 30.1 (MISCELLANEOUS GOODS -- Office Supplies); 45.3
(INFORMATION PROCESSING -- Input Output Units)
JAPIO KEYWORD: R087 (PRECISION MACHINES -- Automatic Banking); R131
(INFORMATION PROCESSING -- Microcomputers & Microprocessors)
JOURNAL: Section: M, Section No. 1110, Vol. 15, No. 178, Pg. 133, May
08, 1991 (19910508)

ABSTRACT

PURPOSE: To ensure that various programs can be selectively obtained for display in response to the operation of a keyboard by providing a touch panel for keyboard placed over a display surface occupying the entire area of an IC card.

CONSTITUTION: An IC card 1 consists of a display surface 2 occupying the entire surface of the card for data display and a touch panel 3 for keyboard placed over the display surface 2. A control circuit is powered by a cell 4. CPU 5 gives various data signals to an automatic deposit payment machine ATM and receives said signals from the machine, through an interface circuit 6. Then the CPU 5 processes these signals in accordance with programs stored in ROM 7 and stores the processed data in RAM 8. If a card user touches key switches 9 of the touch panel 3, data selected is displayed on the display surface 2 by driving a liquid crystal display driver 10 and controlling a crystal liquid display 11. Magnetic stripes 12 are formed on the rear of the IC card 1.

27/5/35 (Item 35 from file: 347)
DIALOG(R)File 347:JAPIO
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03067028 **Image available**
IC MEMORY CARD

PUB. NO.: 02-042528 [JP 2042528 A]
PUBLISHED: February 13, 1990 (19900213)

INVENTOR(s): MIZUTA MASA HARU
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-192668 [JP 88192668]
FILED: August 03, 1988 (19880803)
INTL CLASS: [5] G06F-009/06; G06F-012/14; G06K-019/073
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units); 30.1 (MISCELLANEOUS GOODS -- Office Supplies); 45.2 (INFORMATION PROCESSING -- Memory Units); 45.3 (INFORMATION PROCESSING -- Input Output Units)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessors)
JOURNAL: Section: P, Section No. 1041, Vol. 14, No. 201, Pg. 114, April 24, 1990 (19900424)

ABSTRACT

PURPOSE: To avoid such an inconvenient case where a distribution software is illegally copied by adding a **RAM** chip serving as a temporary memory and an address trap circuit which gives an access to a part of the distribution software with designation of a specific address to an **IC card** containing plural **ROM** chips which **store** the distribution software .

CONSTITUTION: The **ROM** chips 31 and 32 are added to a memory chip part 3 of an **IC** memory **card** together with a **RAM** chip 9 which can read and write data as a temporary memory. A memory address trap circuit 10 is connected to the chip 9 via a trap address line 13. An access of data is carried out to the chip 9 when the input of the circuit 10 indicates a specific address. Then a chip selection circuit 2 is set in an inhibition state by an inverter circuit 11. Thus the reading/writing actions are inhibited to both chips 31 and 32.

27/5/37 (Item 37 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2003 JPO & JAPIO. All rts. reserv.

02994863 **Image available**
PORTABLE INFORMATION STORAGE DEVICE

PUB. NO.: 01-292463 [JP 1292463 A]
PUBLISHED: November 24, 1989 (19891124)
INVENTOR(s): TANAKA TSUTOMU
SHIMIZU WATARU
OBARA TOSHIO
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-122770 [JP 88122770]
FILED: May 19, 1988 (19880519)
INTL CLASS: [4] G06F-015/02; G06F-015/02; G06K-017/00
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 29.4 (PRECISION INSTRUMENTS -- Business Machines); 45.3 (INFORMATION PROCESSING -- Input Output Units)
JAPIO KEYWORD: R011 (LIQUID CRYSTALS); R098 (ELECTRONIC MATERIALS -- Charge Transfer Elements, CCD & BBD); R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessors)
JOURNAL: Section: P, Section No. 1005, Vol. 14, No. 76, Pg. 121, February 13, 1990 (19900213)

ABSTRACT

PURPOSE: To reduce the size and weight of the whole device and to obtain a device with excellent portability and a rapid retrieving speed by storing

image information in an IC memory card , retrieving the stored contents if necessary and displaying the retrieved result.

CONSTITUTION: When an IC memory card 8 is set up and a registration key is depressed at the time of registering image information, an MPU 20 reads out a registration program from a ROM 37 to start operation. After inputting ID information through a keyboard 3, image information is read out by a hand scanner 10. The read image information is binalized and compressed by an image processing part 25, a block number is added to the compressed information and the added information is written in a RAM 38 of the IC memory card 8. When a retrieval key is depressed in case of retrieving the registered image information, a retrieval program is read out from the ROM 37 to start operation and the image information of a corresponding block number is read out on the basis of the inputted ID information and displayed on a liquid crystal display part 2.

27/5/55 (Item 10 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2003 Thomson Derwent. All rts. reserv.

011819254 **Image available**

WPI Acc No: 1998-236164/199821

XRPX Acc No: N98-187277

IC card with exclusive file selection function - has I/O interface used to transmit response information, which corresponds to file selection command received from external, from CPU to external

Patent Assignee: DAINIPPON PRINTING CO LTD (NIPQ)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 10074243	A	19980317	JP 96229558	A	19960830	199821 B

Priority Applications (No Type Date): JP 96229558 A 19960830

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 10074243	A		10 G06K-017/00	

Abstract (Basic): JP 10074243 A

The IC card (10) has a ROM (12), a RAM (14) and an EEPROM (16) that store several exclusive files respectively. When a file selection command is received from an external, one corresponding exclusive file is selected from several exclusive files as a response information by a CPU (18).

The response information is transmitted from the CPU to the external via a I/O interface (19). A reference information, which should be referred when executing the exclusive file selection command, and a basic file relevant to the selected exclusive file are acquired.

ADVANTAGE - Enables efficient utilisation of memory resources, thus offering high-speed service. Enables quick searching of basic file which has control information, thus enabling arbitrary selection of whether control information is included in response of file selection command.

Dwg.1/7

Title Terms: IC; CARD; EXCLUDE; FILE; SELECT; FUNCTION; INTERFACE; TRANSMIT ; RESPOND; INFORMATION; CORRESPOND; FILE; SELECT; COMMAND; RECEIVE; EXTERNAL; CPU; EXTERNAL

Index Terms/Additional Words: READ-ONLY; MEMORY; RANDOM; ACCESS; MEMOYELECTRICALLY; ERASABLE; PROGRAMMABLE; READ-ONLY; MEMORY; INPUT/OUTPUT

File 275:Gale Group Computer DB(TM) 1983-2003/Apr 10
(c) 2003 The Gale Group
File 621:Gale Group New Prod.Annou.(R) 1985-2003/Apr 10
(c) 2003 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2003/Apr 10
(c) 2003 The Gale Group
File 16:Gale Group PROMT(R) 1990-2003/Apr 10
(c) 2003 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
(c) 1999 The Gale Group
File 148:Gale Group Trade & Industry DB 1976-2003/Apr 10
(c)2003 The Gale Group
File 624:McGraw-Hill Publications 1985-2003/Apr 10
(c) 2003 McGraw-Hill Co. Inc
File 15:ABI/Inform(R) 1971-2003/Apr 10
(c) 2003 ProQuest Info&Learning
File 647:CMP Computer Fulltext 1988-2003/Mar W3
(c) 2003 CMP Media, LLC
File 674:Computer News Fulltext 1989-2003/Apr W1
(c) 2003 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2003/Apr 10
(c) 2003 The Dialog Corp.
File 369:New Scientist 1994-2003/Mar W5
(c) 2003 Reed Business Information Ltd.
File 112:UBM Industry News 1998-2003/Apr 11
(c) 2003 United Business Media
? ds

Set	Items	Description
S1	332371	(SMART OR CHIP OR STORED OR CRYPTO OR ACCESS OR SECURITY OR VALUE OR TRANSACTION? ? OR IC OR PAYMENT? ? OR PROGRAMMABLE)-(2W)CARD?? OR INTEGRATED()CIRCUIT? ? OR ELECTRONIC(1W)(PURSE?? OR WALLET?? OR CARD? ?)
S2	13195	(VOLATILE OR UNSTABLE OR NONPERSISTENT OR NON()PERSISTENT - OR TRANSIENT)(3N)(STOR???? OR MEMOR???)
S3	429145	RAM OR RANDOM?()ACCESS()MEMORY OR DRAM OR SRAM OR SDRAM OR RDRAM OR SLDRAM OR SGRAM OR DRDRAM
S4	17867	(NONVOLATILE OR "NON-VOLATILE" OR PERSISTENT OR PERMANENT)-(3N)(STOR? OR MEMOR???)
S5	410917	ROM OR READ()ONLY()MEMORY OR PROM OR EPROM OR EEPROM
S6	44029	(S2:S5 OR MEMOR???) (5N)(FILE? ? OR OBJECT? ? OR DOCUMENT? ? OR CONTENT)
S7	393803	(ACCESS? OR RETRIEV? OR OBTAIN? OR FIND??? OR SEARCH??? OR TRACK???) (5N)(FILE? ? OR OBJECT? ? OR DOCUMENT? ? OR CONTENT)
S8	276317	(TABLE? ? OR DIRECTOR??? OR REPOSITOR??? OR DATABASE? ? OR DATA()BASE? ? OR LIST????) (5N)(FILE? ? OR OBJECT? ? OR DOCUMENT? ? OR CONTENT)
S9	1449	S1(S)S2:S3(S)S4:S5
S10	9	S1(S)S2:S3(S)S4:S5(S)S6(S)S7:S8
S11	181	S2:S3(S)S4:S5(S)S6(S)S7:S8
S12	118	RD (unique items)
S13	112	S12 NOT PD>20001127
S14	12	S1 AND S13
S15	17	S10 OR S14
S16	12	RD (unique items)
S17	127756	(S2:S5 OR MEMOR???) (5N)(DATA OR INFORMATION OR RECORD? ?)
S18	1981310	(ACCESS? OR RETRIEV? OR OBTAIN? OR FIND??? OR SEARCH??? OR TRACK???) (5N)(DATA OR INFORMATION OR RECORD? ?)
S19	1095738	(TABLE? ? OR DIRECTOR??? OR REPOSITOR??? OR DATABASE? ? OR DATA()BASE? ? OR LIST????) (5N)(DATA OR INFORMATION OR RECORD? ?)

S20 29 S1(S)S2:S3(S)S4:S5(S)S17(S)S18:S19
S21 19 RD (unique items)
S22 18 S21 NOT S16

16/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01700449 SUPPLIER NUMBER: 16243842 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Singapore Telecom to introduce payment by smart cashcard after six-month trial, likely in 1996.
Computergram International, CGI08260014
August 26, 1994
ISSN: 0268-716X LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 326 LINE COUNT: 00026

... Pte Ltd six-month pilot study, individuals will be able to leave their cash in the bank and simply carry around a multi-functional rechargeable Smart Card to pay for virtually everything. The **Smart Card** is supplied by Gemplus SA of Gemenos, France. The credit card-sized piece of plastic will be known in Singapore as the CashCard. Gemplus's cards are based on Electrically Erasable and Programmable Memory technology and are known as PCOS **EEPROM**. Each one can hold 32 **directories** each with 255 **files**; it has 1Kb of non-volatile **memory** and 3Kb of **ROM**. The read, write and update facilities can be protected by secret codes. The cards will be issued in denominations worth around \$13, \$33 and \$66. During the trial 40,000 **Smart Cards** will be issued so that Singaporeans will be able to pay the bill at restaurants, telephone calls, car parks and eventually road toll plazas at...

16/3,K/2 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01502697 SUPPLIER NUMBER: 11978677 (USE FORMAT 7 OR 9 FOR FULL TEXT)
The hard edge. (The Tech Section)
Harvey, David A.; Santalessa, Rich
Computer Shopper, v12, n3, p647(4)
March, 1992
ISSN: 0886-0556 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 4795 LINE COUNT: 00359

... adventurous and try something that sends your machine to lock-up land.

Another note: When MAX performs its ROM Search, it adds the areas it **finds** to your PRO file in the form of **RAM** = statements. These are apparently incompatible with VGAswap, and if you try to boot with both statements in the PRO file, MAX will use whichever comes...got other ideas in mind. By starting from the bottom up, we hope to shed some light on the often mysterious connections between BIOS, motherboards, **chip** sets, adapter **cards**, and software. One of the problems with the horizontally of the PC marketplace is that we often operate under the assumption that one machine fits...

16/3,K/3 (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01501253 SUPPLIER NUMBER: 11936304 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Vitesse announcements. (Vitesse Semiconductor debuts VGFX350K application specific integrated circuit, VGFX40K and VGFX20K gate arrays and G-TAXIchip chip set) (Product Announcement)

Computergram International, n1872, pCGI03050011

March 5, 1992

DOCUMENT TYPE: Product Announcement

ISSN: 0268-716X

LANGUAGE:

ENGLISH

RECORD TYPE: FULLTEXT

WORD COUNT: 1098 LINE COUNT: 00087

Vitesse announcements. (Vitesse Semiconductor debuts VGFX350K application specific integrated circuit , VGFX40K and VGFX20K gate arrays and G-TAXIchip chip set) (Product Announcement)

... at 100MHz) or silicon ECL at about 50fJ. The new FX20K and FX40K are aimed at high-speed digital functions such as fast cache and **DRAM** control, error detection and correction, bus control, signal processing, crosspoint or crossbar switching, and real-time data processing and control. With the two new arrays...

...grid array. The FX40K is available in a 184-pin ceramic pin grid array. For full optimisation, customers can choose to embed megacells such as **random access memory** , register files , or custom logic blocks in a base FX array. **Read - only memory** compiler technology is also supported for the FX family, speeding the design cycle for custom **RAM** blocks. In addition, skew of clock signals can be minimised through the use of a optimised clock distribution scheme made for each array in the...

...DESCRIPTORS: Application-Specific Integrated Circuit ;

16/3,K/4 (Item 4 from file: 275)

DIALOG(R)File 275:Gale Group Computer DB(TM)

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01430369 SUPPLIER NUMBER: 10672067 (USE FORMAT 7 OR 9 FOR FULL TEXT)

Palmtop computing: HP & Lotus deliver PC power in 11-ounce palmtop computer. (Lotus Development Corp.) (HP 95LX computer) (product announcement)

EDGE: Work-Group Computing Report, v2, n49, p7(1)

April 29, 1991

DOCUMENT TYPE: product announcement

LANGUAGE: ENGLISH

RECORD TYPE: FULLTEXT

WORD COUNT: 1025 LINE COUNT: 00085

... LaserJet, IBM Proprinter, Epson FX-80 and compatible printers.

With all the built-in software, including Lotus 1-2-3 and MS-DOS executable from **ROM** , most of the computer's 512K of **random - access memory** (**RAM**) is reserved for **file** creation and storage.

In addition, several independent software vendors are expected to release HP 95LX versions of their products on plug-in ROM cards.

Announced...

...helped define PC standards. It includes Intel Corp.'s most highly integrated DOS solution to date, reducing the standard PC/XT chip set from five **integrated circuits** to two. Advanced electronic-design integration allows most of the PC hardware functionality (excluding the microprocessor) to be housed on a single application-specific **integrated circuit** (ASIC).

The HP 95LX is the smallest palmtop PC to include Microsoft Corp.'s MS-DOS ROM (Version 3.22) operating system that is executed...

16/3,K/5 (Item 5 from file: 275)

DIALOG(R)File 275:Gale Group Computer DB(TM)

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01415424 SUPPLIER NUMBER: 09827943 (USE FORMAT 7 OR 9 FOR FULL TEXT)

Minigrams.

Computergram International, n1592, CGI01170018

Jan 17, 1991

ISSN: 0268-716X LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT

WORD COUNT: 2199 LINE COUNT: 00185

... IBM personal computers and compatibles, with pull-down menus, spell-check and thesaurus as well as columns, tables and graphics features; it comes with a **read only memory** card, floppy disks containing install, printer and utility **files**, and a 521Kb **random access memory card** is recommended; the program is available from distributors at #425.

- o -

Frame Technology Corp of San Francisco, California has announced European-language versions of its...

16/3,K/6 (Item 6 from file: 275)

DIALOG(R)File 275:Gale Group Computer DB(TM)

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01311418 SUPPLIER NUMBER: 07397298 (USE FORMAT 7 OR 9 FOR FULL TEXT)

Two chips push PostScript performance. (Talaris Systems uses National Semiconductor and Texas Instrument ICs)

Ferris, Barry

ESD: The Electronic System Design Magazine, v19, n6, p39(4)

June, 1989

ISSN: 0893-2565 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT

WORD COUNT: 3022 LINE COUNT: 00243

... the third is the conversion of text manipulation operators into display list objects.

In addition to interpretation, the 32016 supervises data I/O from ROM, **RAM**, or a SCSI disk. For example, PostScript **files** stored in **RAM** or on the disk drive (such as a Macintosh Laser-Prep **file**, raster data, or forms) are **retrieved** by the 32016 when another PostScript file makes reference to them.

The 32016 also acts as an Intellifont glyph (character) server. For example, when it...

...DESCRIPTORS: **Integrated Circuits**

TRADE NAMES: Talaris Systems PSI (**Integrated circuit**)--

16/3,K/7 (Item 1 from file: 621)

DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

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01161050 Supplier Number: 42024986 (USE FORMAT 7 FOR FULLTEXT)

HP AND LOTUS DELIVER PC POWER IN 11-OUNCE PALMTOP COMPUTER

News Release, p1

April 23, 1991

Language: English Record Type: Fulltext

Document Type: Magazine/Journal; Trade

Word Count: 1288

... IBM Proprinter, Epson FX-80 and compatible printers.

With all the built-in software, including Lotus 1-2-3 and MS-DOS (R) executable from ROM, most of the computer's 512K of **random - access memory** (RAM) is reserved for **file** creation and storage.

In addition, several independent software vendors are expected to release HP 95LX versions of their products on plug-in ROM cards. Announced...

...helped define PC standards. It includes Intel Corp.'s most highly integrated DOS solution to date, reducing the standard PC/XT chip set from five **integrated circuits** to two. Advanced electronic-design integration allows most of the PC hardware functionality (excluding the microprocessor) to be housed on a single application-specific **integrated circuit** (ASIC).

The HP 95LX is the smallest palmtop PC to include Microsoft Corp.'s MS-DOS ROM (Version 3.22) operating system that is executed...

16/3,K/8 (Item 1 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
(c) 2003 The Gale Group. All rts. reserv.

01400512 Supplier Number: 41800797 (USE FORMAT 7 FOR FULLTEXT)
WORDPERFECT UK SAYS THAT WORDPERFECT 5.1 IS NOW AVAILABLE ON A SLOT-IN CARD
FOR THE POQET PC, THE POCKET-SIZED PERSONAL COMPUTER
Computergram International, n1592, pN/A
Jan 17, 1991
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 85

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
...IBM personal computers and compatibles, with pull-down menus, spell-check and thesaurus as well as columns, tables and graphics features; it comes with a **read only memory** card, floppy disks containing install, printer and utility **files**, and a 521Kb **random access memory card** is recommended; the program is available from distributors at GBP425.

16/3,K/9 (Item 1 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)
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01712920
Diskless Workstation Supports Both PC, VAX.
INFOWORLD June 29, 1987 p. 5

... ports, one supporting 19.2 Kbps and one supporting 38.4 Kbps transmission. The computer can store 2 Mbytes of data in a battery-backed **random access memory file**; some 128K of programmable **read - only memory** or 64K of **random access memory** can be **stored** in a **card file**. ...

16/3,K/10 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

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10123406 SUPPLIER NUMBER: 20300374 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Ventures from employee to entrepreneur: countdown to starting your own business.

Vaz, Valarie

Essence, v28, n11, p121(6)

March, 1998

ISSN: 0014-0880

LANGUAGE: English

RECORD TYPE: Fulltext; Abstract

WORD COUNT: 3462 LINE COUNT: 00268

... notebook computer. Desktop models, however, often give you more bang for your buck in terms of memory, built-in accessories and software (see below). Memory. **RAM** (**random - access memory**) determines how fast your computer processes information. Go with at least 32 megabytes. Basic hard drives -- the **permanent** software- **storage** system for computer **files** -- usually offer about 1.6 gigabytes of memory, but 3.2-gigabyte drives are quickly replacing them. Fax and modem. These days a 33.6 possible for you to transmit files to another computer or over the Internet; you'll be able to receive **files** as well. CD- **ROM** drive. Although optional, a CD- **ROM** drive will allow you to display moving video images and use many reference guides and business directories that can help you market your enterprise. Software...

...bundle word-processing, spreadsheets, database and presentation-graphics applications, as well as extras that will allow you to create a business plan, draw up legal **documents** , organize sales contacts and **track** inventory. The most popular: Microsoft Office, Corel WordPerfect Suite 7 and Lotus SmartSuite.

Accounting programs simple enough for the basic computer user, like QuickBooks Pro...

...WORK). An on-line service that's full of practical tips, such as your sales will grow as much as 50 percent if you accept **payment** by credit **card** .

Yahoo!'s Small Business Information (www.yahoo.com/Business...)

16/3,K/11 (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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10087361 SUPPLIER NUMBER: 20435122 (USE FORMAT 7 OR 9 FOR FULL TEXT)
EEPROM: survival of the fittest. (electrically erasable programmable read-onle memory)

Dipert, Brian

EDN, v43, n2, p77(9)

Jan 15, 1998

ISSN: 0012-7515

LANGUAGE: English

RECORD TYPE: Fulltext; Abstract

WORD COUNT: 7133 LINE COUNT: 00581

... that use EEPROM is much longer, including networking equipment, universal remote controls, cordless phones, garage-door openers, cameras, automotive electronics, home audio and video, and **smart cards** . Think about how many devices you use every day that contain some amount of updatable data that remains intact even if you pull the power...Data-read accesses can potentially be faster, because the data-storage portion of the flash memory shares the existing code memory's parallel interface. However, **EEPROM** -emulation software and **file** -format overhead, which are especially slow when you use a linked- **list file** system, may preclude any performance improvement. Also, if the flash memory doesn't allow reads

from the code portion while programming or erasing the data...
...software characterization, delay interrupt servicing as a lower priority function, or selectively block interrupts during data or code updates. You also must include necessary external **RAM** in your design to execute the suspend/resume routine and file-management software.

The other controversial selling point of the "two-in-one" flash memory ...mil SOIC, and a low-profile, 14-lead TSSOP. Several companies also offer EEPROMs in bare-die form, an option that's attractive in ultrathin **smart cards**. Chip-scale packaging, under development by several EEPROM vendors including SGS-Thomson, will soon deliver another ultrasmall alternative, close to die in size but much...both arrays. A fifth 64-bit password restores normal device operation. Xicor also sells the X76F128, as well as other product-family members, in a **smart - card** form factor.

Taking advantage of its European presence and the **smart - card** popularity in that part of the world, SGS-Thomson has focused on highly secure EEPROMs. The ST13xx families, intended for prepaid phone-card usage, contain several distinct subarrays, hardwired security logic and fuses, and an optional authentication secret key. Atmel and Microchip Technology also supply **smart - card** and RFID ICs (Reference 6). Atmel's AT88SC10X devices keep track of the number of incorrect security-code attempts and permanently invalidate the memory after...real-time-clock, and watchdog-timer functions; 8 ISA plug-and-play controllers; 9 VESA plug-and-play memories; 10 Secure EEPROMs, encryption chips, and **smart - card** ICs; 11 Serial-presence-detection memories; 12 FPGA configuration memories.

References

1. Dipert, Brian, "FRAM: ready to ditch niche?" EDN, April 10, 1997, pg 93...

16/3,K/12 (Item 3 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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03900654 SUPPLIER NUMBER: 07164420 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Smart cards are getting smarter faster.
Terry, Chris
EDN, v34, n6, p69(4)
March 16, 1989
ISSN: 0012-7515 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1856 LINE COUNT: 00144

Smart cards are getting smarter faster.

ABSTRACT: **Smart cards** are beginning to appear in an increasing number of applications, including electronic instrumentation, process control, diskless computers for harsh environments, and re-configurable intelligent peripheral devices, such as printers and point-of-sale terminals. Demand for both memory and microcontroller **smart cards** is growing due to the the greater availability of faster, more powerful cards. Memory cards with capacities ranging from 8Kbytes to 2Mbytes are readily available...

...3Kbytes to 6Kbytes of mask ROM to hold the operating system and application program, and 2Kbytes to 16Kbytes of EEPROM to hold user data. Several **smart cards** are profiled.

TEXT:

Smart cards are getting smarter and faster

A few years ago, when credit-card-size memory cassettes and microcontrollers (**smart cards**) first became reliable, many observers predicted that the miniature cards would become an immediate success and

quickly replace magnetic-stripe cards. **Smart cards** didn't proliferate as soon as expected, but they're now beginning to appear in an increasing number of applications, including electronic instrumentation, process control, diskless computers for harsh environments, and reconfigurable intelligent peripheral devices, such as printers and point-of-sale terminals. Because **smart cards** are getting faster and more powerful, the demand for both the memory and the microcontroller cards is growing steadily. Epson, for example, is now delivering nearly 50,000 memory cards per month, compared with 15,000 per month in mid-1987.

Frank Gruppuso, senior vice president of technology development at **Smart - Card International Inc.**, points out that in this country, the universal use of magnetic-stripe ATM (automatic teller machine) cards occurred only in the last few...

...cards, readers, and software is so great that the United States' banking industry won't quickly switch to other methods. More likely, he concludes, the **smart - card** technology will gradually penetrate the financial world, and the two technologies will exist concurrently for a while.

This gradual transition is already apparent in France and Japan, where **smart cards** are used for general financial purposes. Visa is experimenting with **smart cards** in a pilot project that embraces cash advances and point-of-sale credit transactions. Further, a machine currently under development speeds up the credit-card verification procedure by checking your credit card against a list of invalid numbers contained in an EEPROM **smart card**. The machine eliminates the need to phone an authorizing agency, and a built-in modem allows the retailer to update the list by downloading the latest version of the list from the authorizing agency's computer.

The memory-type **smart cards** may even relegate bubble memory--once touted as the ideal storage medium for harsh environments--to the status of "an interesting idea that didn't make it." Compared with bubble memory, **smart cards** take up far less space, are much faster (their 150-to 300-nsec access time compares to the millisecond access times of bubble memory) and...

...via a serial link costs \$960, and an adapter that plugs into Data I/O or Stag programmers costs \$150.

A recent entry into the **smart - card** field is Fujisoku, which first began developing **smart cards** in 1982. This vendor now distributes its products in the United States through Shigma Inc. Its cards feature static RAM, EEPROM, EPROM, one-shot PROM...

...or mask ROM. Prices vary from \$18 for 8k bytes of static RAM to \$98 for 1M byte of mask ROM (5000).

Other suppliers of **smart memory cards** include Dallas Semiconductor (Dallas, TX), Du Pont Connector Systems (New Cumberland, PA), and Mitsubishi Electronics America Inc (Sunnyvale, CA); their products are described in an...International Inc comply with these various configuration constraints. The units have an 8-bit architecture and contain a low-power CMOS processor, 128 bytes of **RAM** workspace, 3k bytes of **ROM**, and 2k bytes of **EEPROM**. The software contained in the **ROM** not only provides a multilevel security structure guarded by password, PIN, or key access protocols, but also lets you partition the data memory to hold multiple, independent data sets. Each data set can have its own security level and access method. The **ROM**-resident operating system is responsible for the low-level storage and retrieval of data within the **EEPROM**; the card reader can **access files** by name alone and does not have to handle physical memory addresses.

The microcontroller cards conform to the ISO standards for size (85X54X0.76 mm...

22/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01513541 SUPPLIER NUMBER: 12197197 (USE FORMAT 7 OR 9 FOR FULL TEXT)
PC-Card standard release 2.0 unleashes a myriad of applications. (Personal Memory Card International Association's new standards for memory cards) (includes related article on the Personal Memory Card International Association) (Technical)
Nass, Richard
Electronic Design, v40, n2, p45(6)
Jan 23, 1992
DOCUMENT TYPE: Technical ISSN: 0013-4872 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 3866 LINE COUNT: 00303

... for random error because the intrinsic error rate inb a system that's properly designed is quite low.

THE LAYERED METAFORMAT

The first peice of **information** contained in each card's **memory** is a metaformat header that describes the card's data organization, including both hardware and software. The metaformat is organized in four layers. The basic compatibility layer contains only the minimal information needed to **access** the **card**, such as device speed, type, and size, as well as a programming algotithm if it's required. The second layer, the data-format layer, specifies...

...a bunch of data with no higher-level organization) are supported, as well as CRC and other types of error detection. Mixex-format cards like **ROM** and **RAM** are allowed. In the **data** -format level, nothing is DOS-specific.

The third level, the data-organization layer, is DOS-specific. Here, the defined file system can be the file...

22/3,K/2 (Item 2 from file: 275)
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01487355 SUPPLIER NUMBER: 12760206
Compass offers family of retargetable libraries. (Compass Design Automation's Liberty Series of physical layouts for integrated circuits) (Product Announcement)
Goering, Richard
Electronic Engineering Times, n715, p14(2)
Oct 19, 1992
DOCUMENT TYPE: Product Announcement ISSN: 0192-1541 LANGUAGE: ENGLISH
RECORD TYPE: ABSTRACT

ABSTRACT: Compass Design Automation has introduced the Liberty Series, a range of retargetable libraries of physical layout designs for **integrated circuits** (ICs). The software, priced at between \$100,000 and \$1 million, generates characterized layout libraries and is intended to reduce the time IC designers spend constructing libraries to model new processes. Creating libraries is currently a major expense for producers of application-specific **integrated circuits** (ASICs) and custom **integrated circuits**. The product is centered on compilers and ASIC libraries that Compass's parent company, VLSI Technology, originally developed. This core includes compilers for **read - only memory (ROM)**, **random - access memory (RAM)** and multiplier cells; a **data** -path compiler; net- list

compilers for multiplier, multiplier-accumulator and data-path applications; a gate-array library of 265 macros; and a standard-cell library of 265 cells.

22/3,K/3 (Item 3 from file: 275)
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01369559 SUPPLIER NUMBER: 08805618 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Patent award stuns chip manufacturers; impact still unclear. (Gilbert Hyatt, father of the microprocessor)
Burke, Steven
PC Week, v7, n35, p1(2)
Sept 3, 1990
ISSN: 0740-1604 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 423 LINE COUNT: 00033

ABSTRACT: Computer engineer Gilbert Hyatt has received a patent that names him father of the microprocessor. Hyatt originally filed for a patent for the 'single chip **integrated circuit** computer architecture' on Dec 28, 1970; the patent was approved on Jul 17, 1990. Patent attorneys maintain that such a long examination time is unusual...

...the type of microprocessor it covers. The Hyatt patent is believed to cover any microprocessor that uses read-only memory (ROM) for storing microcode and **random - access memory (RAM)** for storing register information .

22/3,K/4 (Item 4 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01013289 SUPPLIER NUMBER: 00610637
Exploring the Memory Jungle.
Pearlman, D.
Popular Computing, v2, n8, p204-206
June, 1983
ISSN: 0279-4721 LANGUAGE: ENGLISH RECORD TYPE: ABSTRACT

ABSTRACT: Computer memory is a measure of the capacity to store **information** . The more **memory** a computer has, the more **information** can be processed at one time. Kbytes are used to measure internal memory in powers of two because the basic component is an on-off switch. Random access is a new and faster method than sequential **access** to **information** in **memory** . The **memory** is usually on **integrated circuit** chips inside the computer, called internal memory. External memory refers to floppy disks, hard disks, or cassette tapes. **RAM** , **ROM** , and **PROM** are types of internal memory.

22/3,K/5 (Item 1 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)
(c) 2003 The Gale Group. All rts. reserv.

01397818 Supplier Number: 46493135 (USE FORMAT 7 FOR FULLTEXT)
INTEGRATED SILICON SOLUTION, INC. ANNOUNCES JOINT VENTURE WITH TSMC
PR Newswire, p0625SFTU052
June 25, 1996

Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 464

... board and CEO of WaferTech. Kenneth G. Smith, a former Micron executive, has been appointed President and COO.

ISSI designs, develops and markets high performance **SRAM** and **nonvolatile memory integrated circuits** (FLASH, **EPROM**, **EEPROM**) used in networking, telecommunications, **data** communications, personal computers, instrumentation and consumer products. ISSI is an international firm with its headquarters in Sunnyvale, CA. Its global infrastructure includes subsidiaries in Taiwan, Hong Kong, and the People's Republic of China. More **information** can be **obtained** from the company's SEC filings.

This press release contains forward looking statements including, but not limited to, anticipated schedules and wafer volumes. Actual production ...

22/3,K/6 (Item 2 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)
(c) 2003 The Gale Group. All rts. reserv.

01384268 Supplier Number: 46401380 (USE FORMAT 7 FOR FULLTEXT)
MARS ELECTRONICS INTERNATIONAL SIGNS WORLDWIDE AGREEMENT WITH DIGICASH
PR Newswire, p520PHM005
May 20, 1996
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 509

Both Mars Electronics International and DigiCash have been working together to develop and manufacture **Smart Card** readers. **Smart Cards** are, in effect, small computers on credit cards that contain a microprocessor, **Read Only Memory (ROM)** for program storage, **Random Access Memory (RAM)** for **data** storage, and an **EEPROM** (Electronic Erasable Programmable **Read Only Memory**) for **permanent data storage**. "The cards are the cornerstone for new cashless payment systems that are being developed by financial institutions around the world," says Nick Habgood, marketing manager at Mars Electronics, United Kingdom. "**Smart Cards** can be used to develop cashless payment systems that are very secure and very reliable."

The licensing agreement allows MEI to develop a new product...

22/3,K/7 (Item 1 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
(c) 2003 The Gale Group. All rts. reserv.

04091768 Supplier Number: 53867566 (USE FORMAT 7 FOR FULLTEXT)
MAGRAM Decreases Power Consumption.
Energy Conservation News, v21, n6, pNA
Jan 19, 1999
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 226

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
...that will allow the future manufacturing of low-cost, high-volume, high-density memory devices and circuits. The new memory cell, called a

MAGRAM (MAGnetic Random Access Memory), uses magnetic fields to store data . Similar to conventional RAM memory devices, the MAGRAM should allow rapid, random access to information stored within it. However, unlike conventional RAM , the MAGRAM memory cell is nonvolatile - that is, continuous power is not required to maintain the memory content. Even after the power source is removed, the information remains, giving MAGRAM the...

...computers and other electronic devices that use memory. Among potential applications are cellular phones, pagers, palm PCs, digital clocks, microwaves, VCRs, answering machines, calculators, and integrated circuits in vehicles. Contact: Stephen Fleming; Tel: 505/471-3027, ext. 101; Email: sfhfram@newmexico.com.

22/3,K/8 (Item 2 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
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03730621 Supplier Number: 48065073 (USE FORMAT 7 FOR FULLTEXT)
Matsushita, Motorola to team up on noncontact IC card
Japan Semiconductor Scan, pN/A
Oct 20, 1997
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 195

... products divisions will jointly develop a semiconductor chip using Matsushita Electronics' next-generation memory, FeRAM, and Motorola's microcomputer, the sources said.

FeRAM, or ferroelectric random access memory , requires less time for data exchange and lower voltage than commonly used memories for IC cards , such as EEPROM , or electrically erasable programmable read - only memory , the sources said. It runs at 20 times the speed and has a memory capacity 10 times greater, they said.

Shipments of the chip will...

22/3,K/9 (Item 3 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
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03397899 Supplier Number: 46993097 (USE FORMAT 7 FOR FULLTEXT)
Toshiba Announces Low-Cost Smart Card 12/23/96
Newsbytes, pN/A
Dec 23, 1996
Language: English Record Type: Fulltext
Document Type: Newswire; General Trade
Word Count: 332

... tickets, storing credits in dividend cards, leisure activities, and communications, suggested Toshiba.

The CZ-3018 is part of the company's CZ-3000 range of smart cards and has an 8-bit CPU (central processing unit) in addition to a six kilobytes read - only memory and the 128 byte random access memory . It also supports enhanced data security and meets both the ISO/IEC7816 and the EMV (Europay, Mastercard, Visa) standards.

A large potential market for smart cards appeared this year in...

22/3,K/10 (Item 4 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
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01956335 Supplier Number: 43471455 (USE FORMAT 7 FOR FULLTEXT)
ICs For Smart Card Market
Semiconductor Industry & Business Survey, v14, n16, pN/A
Nov 23, 1992
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 757

... Radio Frequency Identification ASICs:
Atmel's nonvolatile, mixed signal ASICs are specifically targeted for the contactless, RF ID market place. These RF ID ASICs combine **nonvolatile memory**, digital logic, and analog circuitry on a single chip to meet the requirements of non-volatile **data storage** and **retrieval** products. These monolithic devices can be packages in contactless **smart cards** and electronic keys, tokens, and tags for monetary value applications. Applications include road tolls, parking, mass transit, ID tags, and vending machines.
Atmel is currently...

22/3,K/11 (Item 5 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
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01388923 Supplier Number: 41766632 (USE FORMAT 7 FOR FULLTEXT)
SMART CARDS BEGINNING TO MAKE MONEY
Data Storage Report, pN/A
Jan, 1991
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 788

... SLE 4402 is reprogrammable, thus allowing the telephone company to reset the count in the EEPROM.

Smart card identifies user

The newer product in the **smart card** category is one with its own microcontroller. Examples of this include the recently announced ST16XYZ family from SGS Thomson. It contains an 8-bit CPU...

...CPU executes programming that control all card operations. It hides the relationship between memory contents and the supply voltage to prevent unauthorized examination of the **memory** contents. It restricts **data access** across the various **memories**, **ROM**, **RAM**, and **EEPROM**. And it provides interrupt upon detection of unauthorized access.

The chip comes with onchip ROM, RAM and EEPROM. ROM can be vary from 512 bytes...

22/3,K/12 (Item 6 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
(c) 2003 The Gale Group. All rts. reserv.

01181676 Supplier Number: 41067082 (USE FORMAT 7 FOR FULLTEXT)
FUJI SHOWS SECOND GENERATION STILL VIDEO CAMERAS, THOUGH MARKET YET TO HEAT UP
Video Technology Newsletter, v2, n24, pN/A

Dec 18, 1989

Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 356

... t stopped Fuji Photo Film and Toshiba from forging ahead on second generation models of a new still video format--digital cameras that use an **integrated circuit (IC) card** in place of a floppy disk to record images. In Fuji's DP- 1P, image **information** is stored on static **random access memory (SRAM)** chips before being transferred to a **permanent storage** medium like an optical disk. The breakthrough in IC technology--which Fuji has been working on for 10 years--was the development of large-scale...

22/3,K/13 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2003 The Gale Group. All rts. reserv.

04191789 Supplier Number: 46127161
Ramtron International - Company Report
Investext, pl-5
Feb 5, 1996
Language: English Record Type: Abstract
Document Type: Magazine/Journal; Trade

ABSTRACT:

...Ramtron uses its memory design expertise to explore opportunities for proprietary designs of conventional memory chips (EDRAMs, enhanced DRAMs). A major opportunity will be the **smart card** /tag (RF ID) market, where Ramtron's FRAMs are a driving force. Ramtron's breakthrough ferroelectric **RAM (FRAM)** chips provide low-cost, low-power, high-speed, read/write, **nonvolatile memory** chips (**data** is remembered after the power is removed). The chips run without a battery; power comes directly from a tiny antenna wrapped around a credit card...

...energized by a radio signal; capacitative coupling with the chip provides the power). The result is a highspeed (2K bits per second), read/write, batteryless **smart card** that is the size of a credit card. Tables in report: Stock Price And Earnings **Data** 1995-97 The INVESTEXT **database** offers the full text of this report online (RN=1698716). To order printed copies, CALL (800)662-7878, (212)484-4700 US, (071)815-3860...

22/3,K/14 (Item 1 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)
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01756940
ITT CANNON AND TOPPAN PRINTING CO., LTD. AGREE TO DEVELOP A LINE OF IC MEMORY CARDS
News Release August 3, 1987 p. 1

ITT Cannon and Toppan Printing Co., Ltd. announced today a licensing agreement for joint development of **IC memory cards** to be called the ITT Cannon STAR Card. About the size of a credit card, this add-on memory device is a reliable, fast and highly portable alternative to floppy disks, memory cartridges or internal system memory chips. Toppan, developer of Japan's first **IC card** (or " **smart** " **card**), together with ITT Cannon, developer of the world's first connector, jointly designed an **IC Memory**

Card for use in applications where high speed digital **information** storage and **retrieval** is needed. Major components of the system include the IC's, a lithium battery and a new PCB-style connector designed by ITT Cannon Japan. Protection is provided by a molded frame and top and bottom panels. The ITT Cannon STAR Card introduced by ITT Cannon and Toppan, features both **RAM** (S- **RAM**) and **ROM** (MASK **ROM** , OTPROM, **EPROM** and **EEPROM**) memory alternatives. **ROM** allows the card to extract **data** , whereas **RAM** **memory** allows the card to exchange **data** . A high-speed direct **access** capability allows much faster processing of **information** than conventional **memory** devices. This IC Memory **Card** is up to 1,000 times faster than a floppy disk and unlike the floppy disk, is not susceptible to dust or other environmental contaminants...

22/3,K/15 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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10222165 SUPPLIER NUMBER: 20641310 (USE FORMAT 7 OR 9 FOR FULL TEXT)
IC Advances Share The Spotlight With New Products At CeBIT 98.
Vollmer, Alfred
Electronic Design, v46, n11, p72(1)
May 13, 1998
ISSN: 0013-4872 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 3004 LINE COUNT: 00238

TEXT:

...systems. For example, Siemens Nixdorf Informationssysteme AG of Munich, Germany presented its Scenic Mobile 800, a notebook PC that does more than just offer a **chip - card** reader for increased security, and a removable keyboard with an IR link to the notebook PC for increased comfort. It also is equipped with an...

...coded audio data. Both devices exhibited very good music playback, which is claimed to be of CD quality. However, while Pontis' MPlayer3 uses an exchangeable **ROM** or Flash MMC (see ELECTRONIC DESIGN, March 28, 1998, p. 102) for music storage, Saehan's MPman has a built-in flash memory, which is...

...software, which Philips Semiconductors developed with Silicon & Software Systems (S3), Dublin, Ireland (www.s3group.com), implements all the data-communications tasks involved, including the DECT **data** protocol, link- **access** protocol, and V.24 UART interfacing to the host computer. Speakerphone ICs Another CeBIT announcement from Philips Semiconductors is the PCD600H, which integrates all the...

...minutes of voice data, if a 5.2-kbit/s compression rate is selected. With a 2.6-kbit/s rate, 26 minutes of voice **data** can be stored. If the **memory** fills up, the previously stored voice data can be recoded so that more messages can be stored. The DSP also allows fast or slow message... acoustic echo cancellation is that the echo is so long that a relatively high number of taps is needed for additional filters. This requires more **RAM** and **ROM** . A reference design as well as the API are also available. The reference board displayed at CeBIT used 64 kwords (128 kbytes) of flash memory...

...should be used by just programming another flash driver into the OTP. With a purely DSP-based solution, the DSP would run from a maskprogrammable **ROM** . As a result, there's a time delay of several weeks if another flash version is to be used. Another speakerphone solution at CeBIT came...

22/3,K/16 (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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09646866 SUPPLIER NUMBER: 17934224 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Smart cards: trained for security. (includes related articles) (Cover Story)
Gallant, John
EDN, v40, n24, p34(6)
Nov 23, 1995
DOCUMENT TYPE: Cover Story ISSN: 0012-7515 LANGUAGE: English
RECORD TYPE: Fulltext; Abstract
WORD COUNT: 2451 LINE COUNT: 00195

... the correct transport code, on the other hand, allows the manufacturer to load the chip's EEPROM with the desired number of value units.

Additional security for smart cards stems from the way smart-card ICS' (Mu)Cs allocate memory. Each type of memory performs a different function. Volatile RAM serves only as a scratchpad to perform calculations. The ROM stores programs and runs a card's operating system. EEPROM, containing user data, account numbers, and keys, has two sections -- a secure section and a section that a card terminal can access to download application data. Once the secure EEPROM area has its appropriate data loaded, the smart-card manufacturer can blow on-chip fuses to make that section inaccessible. In effect, the secure EEPROM area becomes OTP ROM.

Crypto-cards and coprocessors

One of Siemens' large smart-card ICs is the SLE44C200, an 8-bit crypto-controller. This chip contains an 8-bit...of RAM, 12,800 bytes of ROM, and 4096 bytes of EEPROM, plus an on-chip charge pump for EEPROM programming.

From SGS-Thomson, a smart-card IC supplier since 1982, the top-of-the-line security chip is the ST16CF54. The chip has an 8-bit (Mu)C, 16 kbytes of...

...bits, in software. To guard against fraudulent access, both ROM and EEPROM are configurable into two sectors. A customer-specified memory-access-control matrix establishes access rules for transferring data from any memory section to any other.

Hitachi, another player in smart-card chips, has a special version of its H8/310 (Mu)P, the H8/3102, in...

22/3,K/17 (Item 3 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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06204450 SUPPLIER NUMBER: 13606324 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Smart cards from a manufacturing point of view.
Baker, Tim
Solid State Technology, v35, n10, p65(4)
Oct, 1992
ISSN: 0038-111X LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 1779 LINE COUNT: 00141

... carry a commercial message, each smart card project requires an individual graphic design, which will strongly influence user acceptance.

The Manufacturing Process
Integrated Circuit Types

Integrated circuits for smart cards are manufactured with industry standard technologies. Early smart card ICs used NMOS EPROM technology, but the current trend is toward the use of low power CMOS EEPROMs. Two main IC categories are employed: a) small memory circuits with additional logic to provide simple security systems and b) microprocessor-based circuits with ROM, RAM, EEPROM, and additional circuitry for increased security and more demanding applications. The additional circuitry of the latter prevents unauthorized accessing of the information stored in the EEPROM. For instance, it prevents the circuit from working outside a normal frequency range and it may even be designed to lock up if the protective...

22/3,K/18 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2003 CMP Media, LLC. All rts. reserv.

01022154 CMP ACCESSION NUMBER: WIN19940601S1885
Mobile Mail Keeps Remote Users in the Loop (E-Mail Software)
Hailey Lynne McKerry
WINDOWS MAGAZINE, 1994, n 506 , 076
PUBLICATION DATE: 940601
JOURNAL CODE: WIN LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: New Products

TEXT:

... Pick lists guide you in setting the communications type, serial port parameters, baud rates and dialing options for each location. The program supports long-distance access and credit-card calling. You can select as many as eight communications methods per location, from among such protocols as IPX/SPX (NetWare), TCP/IP (UNIX) and X.25. cc:Mail Mobile also supports connections via ISDN, PBX, direct connection, RAM Mobile Data, cellular and landline modems. The package includes scripts for more than 70 popular modems and supports background operation. A preview function lets you gather information...

...s document retrieval and storage tool, brings up a document log that lists scheduled and concluded faxes. FaxTracker can also display the results of a search and provides specific fax information, such as the file name, type and size. FaxWorks Pro LAN features automatic Group 4 compression and supports up to eight fax lines per fax...sent via popular e-mail messaging protocols, such as MAPI (Microsoft Mail), VIM (Lotus's cc: Mail and Notes) and CMC. The fuzzy logic global search capability can find information even if you're unsure of the spelling. Version 2.1 includes a report formatter for altering the width and height of items on a...

...single screen. You can drag and drop information between related elements (people, documents or activities) or use the QuickLink button to associate different types of information. CrossTies can store and track information about people in 30 preformatted fields, or in a notes field. You can define templates to prefill fields with standard information and place frequently used...deductions, additions and tips. Tips can be recorded by allocated tips or tips in addition to gross pay. Instinctive Payroll also lets you issue and track payroll advances. Instinctive Payroll prints information on preprinted forms on tractor-fed or laser-printer checks. It also includes electronic tax filing to transfer tax deposits directly to the bank. DacEasy...in the background, or cut and paste it into e-mail (depending on the terms of the news

service). You can set up to 32 **search** criteria on topics such as **information** technology and sort the news you receive into different windows according to topic. Mainstream Newscast Price: Software, \$995; FM receiver, \$495; satellite dish, \$990 Contact...

...antiglare, antistatic coating. VisionMaster 17 Price: \$799 Contact: Idek Iiyama North America, 800-394-4355, 215-957-6543 Circle Inquiry 593 Multimedia Kits Include CD- **ROM** Library Procom Technology's Multimedia CD Station and Multimedia Station Pro upgrade kits include a double- speed CD- **ROM** drive with a 320ms average **access** time and a 300KBps **data** -transfer rate. A Media Vision 16-bit sound card with 16-bit stereo recording and playback at 44kHz is also included. The CD Station includes four CD- **ROM** titles (Compton's Interactive Encyclopedia, Dune, Curse of Enchantia and Photo Factory) and Fujikon SP-404 speakers. The Station Pro comes with eight CD-ROMs...

File 8: Ei Compendex(R) 1970-2003/Mar W5
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File 35: Dissertation Abs Online 1861-2003/Mar
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File 144: Pascal 1973-2003/Mar W5
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File 434: SciSearch(R) Cited Ref Sci 1974-1989/Dec
(c) 1998 Inst for Sci Info
File 34: SciSearch(R) Cited Ref Sci 1990-2003/Apr W1
(c) 2003 Inst for Sci Info
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(c) 2003 FIZ TECHNIK
File 438: Library Lit. & Info. Science 1984-2003/Feb
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? ds

Set	Items	Description
S1	477502	(SMART OR CHIP OR STORED OR CRYPTO OR ACCESS OR SECURITY OR VALUE OR TRANSACTION? ? OR IC OR PAYMENT? ? OR PROGRAMMABLE) - (2W)CARD?? OR INTEGRATED()CIRCUIT? ? OR ELECTRONIC(1W)(PURSE?? OR WALLET?? OR CARD? ?)
S2	7123	(VOLATILE OR UNSTABLE OR NONPERSISTENT OR NON()PERSISTENT - OR TRANSIENT)(3N)(STOR???? OR MEMOR???)
S3	121873	RAM OR RANDOM?()ACCESS()MEMORY OR DRAM OR SRAM OR SDRAM OR RDRAM OR SLDRAM OR SGRAM OR DRDRAM
S4	11397	(NONVOLATILE OR "NON-VOLATILE" OR PERSISTENT OR PERMANENT) - (3N)(STOR? OR MEMOR???)
S5	128397	ROM OR READ()ONLY()MEMORY OR PROM OR EPROM OR EEPROM
S6	14903	(S2:S5 OR MEMOR???) (5N) (FILE? ? OR OBJECT? ? OR DOCUMENT? ? OR CONTENT)
S7	128856	(ACCESS? OR RETRIEV? OR OBTAIN? OR FIND??? OR SEARCH??? OR TRACK???) (5N) (FILE? ? OR OBJECT? ? OR DOCUMENT? ? OR CONTENT)
S8	74008	(TABLE? ? OR DIRECTOR??? OR REPOSITOR??? OR DATABASE? ? OR DATA()BASE? ? OR LIST????) (5N) (FILE? ? OR OBJECT? ? OR DOCUMENT? ? OR CONTENT)
S9	2376	S1 AND S2:S3 AND S4:S5
S10	5	S9 AND S6 AND S7:S8
S11	63286	(S2:S5 OR MEMOR???) (5N) (DATA OR INFORMATION OR RECORD? ?)
S12	833152	(ACCESS? OR RETRIEV? OR OBTAIN? OR FIND??? OR SEARCH??? OR

TRACK???) (5N) (DATA OR INFORMATION OR RECORD? ?)
 S13 443026 (TABLE? ? OR DIRECTOR??? OR REPOSITOR??? OR DATABASE? ? OR
 DATA()BASE? ? OR LIST????) (5N) (DATA OR INFORMATION OR RECORD?
 ?)
 S14 40 S9 AND S11 AND S12:S13
 S15 44 S10 OR S14
 S16 43 RD (unique items)
 S17 39 S16 NOT PY=2001:2003
 S18 14373 SMART()CARD? ?
 S19 85 S7 AND S18
 S20 11 S19 AND (S2:S5 OR MEMOR???)
 S21 9 RD (unique items)
 S22 41 S18 AND (FILE() (MANAG? OR SYSTEM? ?) OR FILE? ? (3N) DIRECTO-
 R???)
 S23 35 RD (unique items)
 S24 23 S23 NOT (PY=2001:2003 OR S17 OR S21)

17/5/2 (Item 2 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
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04472419 E.I. No: EIP96083285569
Title: Integrated circuits for smart cards
Author: Krueger, Julie
Corporate Source: Siemens Components, Inc
Conference Title: Proceedings of the 1995 27th International SAMPE
Technical Conference
Conference Location: Albuquerque, NM, USA Conference Date:
19951009-19951012
E.I. Conference No.: 45125
Source: International SAMPE Technical Conference v 27 1995. p 1168-1171
Publication Year: 1995
CODEN: ISTCEF
Language: English
Document Type: JA; (Journal Article) Treatment: G; (General Review)
Journal Announcement: 9610W3

Abstract: Over the past 10 years, three primary factors have driven the semiconductor technology to where it is today: 1) Increased processing power required by personal computers and workstations 2) Increased memory capacity required for massive data storage 3) Lower power ICs required for portable computing and mobile office products The resulting semiconductor technology is ideally suited for smart card integrated circuits (ICs). Since every smart card IC (also known as chip card IC) contains both digital circuitry and nonvolatile memory, advances in these two areas are critical to providing reliable, cost-effective chips for the evolving smart card market. In addition to discussing these trends in more detail, this paper also reviews 1) the types of smart card ICs available, 2) security features of smart card ICs, 3) preparing ICs for insertion into plastic cards, and 4) smart card IC suppliers.

Descriptors: Digital integrated circuits ; Smart cards ; Semiconductor device manufacture; Microprocessor chips; Cost effectiveness; Marketing; Security of data ; ROM ; CMOS integrated circuits ; Random access storage

Identifiers: Memory capacity; Nonvolatile memory ; Electrically erasable programmable read only memory ; Banking applications; Flash memory; Ferroelectric random access memory

Classification Codes:

714.2 (Semiconductor Devices & Integrated Circuits); 911.2 (Industrial Economics); 911.4 (Marketing); 723.2 (Data Processing); 722.1 (Data Storage, Equipment & Techniques); 723.1 (Computer Programming)

714 (Electronic Components); 911 (Industrial Economics); 723 (Computer Software); 722 (Computer Hardware)

71 (ELECTRONICS & COMMUNICATIONS); 91 (ENGINEERING MANAGEMENT); 72 (COMPUTERS & DATA PROCESSING)

17/5/7 (Item 7 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
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03438632 E.I. Monthly No: EI9206076627
Title: IC - card spec adapts I/O to memory-card slot.
Author: Nass, Richard
Source: Electronic Design v 40 n 2 Jan 23 1992 7p
Publication Year: 1992
CODEN: ELODAW ISSN: 0013-4872

Language: English
Document Type: JA; (Journal Article) Treatment: A; (Applications); G;
(General Review)

Journal Announcement: 9206

Abstract: Recent technology breakthroughs in the plug-in IC card arena promise to impact all segments of the computing industry, from portable systems to high-end workstations, including test-and-measurement equipment. Last September saw a major stride taken in this direction when the Personal Computer Memory Card International Association (PCMCIA) introduced Release 2.0 of the PC Card Standard. The standard was jointly accepted by the PCMCIA and the Japanese Electronics Industry Development Association. Release 2.0 is divided into three parts: electrical (interface), physical, and software. Six different types of chips are outlined for use in the cards: ROM, one-time programmable ROM, static RAM, UV EPROM, flash EPROM, and EEPROM. One of the keys to Release 2.0 is that it introduces new applications in the form of I/O cards. This article discusses the standard in detail and includes the PCMCIA-card pin configuration and a flow chart for the MB86301 memory-card controller (Fujitsu). A discussion of the modem on a card is presented to illustrate one application of the standard.

Descriptors: INTEGRATED CIRCUITS --*Standards; MODEMS--Research; COMPUTER HARDWARE--Standards; DATA STORAGE, DIGITAL--Random Access ; DATA STORAGE, DIGITAL-- PROM ; DATA STORAGE, DIGITAL -- ROM

Identifiers: PERSONAL COMPUTER MEMORY CARD INTERNATIONAL ASSOCIATION RELEASE 2.0; PLUG IN INTEGRATED CIRCUIT CARDS; COMMUNICATIONS ON A CARD ; MICROCONTROLLERS; EXCHANGEABLE CARD ARCHITECTURES; MB86301 MEMORY CARD CONTROLLERS

Classification Codes:

713 (Electronic Circuits); 714 (Electronic Components); 723 (Computer Software); 718 (Telephone & Line Communications); 721 (Computer Circuits & Logic Elements); 722 (Computer Hardware)

71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING)

17/5/8 (Item 8 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
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02276776 E.I. Monthly No: EIM8710-065751

Title: MICROPROCESSOR WITH 2 KBYTES EEPROM FOR DATA SECURITY APPLICATIONS.

Author: Nakamura, Hideo; Sawase, Terumi; Kihara, Toshimasa; Matsubara, Kiyoshi

Corporate Source: Hitachi Central Research Lab, Tokyo, Jpn

Conference Title: 1987 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, First Edition.

Conference Location: New York, NY, USA Conference Date: 19870225

Sponsor: IEEE, Solid-State Circuits Council, New York, NY, USA; IEEE, New York Section, New York, NY, USA; University of Pennsylvania, Philadelphia, PA, USA

E.I. Conference No.: 10107

Source: Digest of Technical Papers - IEEE International Solid-State Circuits Conference 1987. Publ by Lewis Winner, Coral Gables, FL, USA. Available from IEEE Service Cent (Cat n 87CH2367-1), Piscataway, NJ, USA p 194-195, 391

Publication Year: 1987

CODEN: DTPCDE

Language: English

Document Type: PA; (Conference Paper)

Journal Announcement: 8710

Abstract: An electrically erasable and programmable microcomputer with security-enhanced architecture is described. The microcomputer consists of functional modules of an 8-b CPU, a 128-b **RAM**, a 4-Kb **ROM**, and a 2-Kb **EEPROM**. A module-based structure is used to satisfy both data security and chip testability. Each module in the chip is isolated from other modules in the module-level test. Security-check circuits for the **ROM** and **EEPROM** prevent undesirable **access** of **data** on the chip during test. Test ports become available on module-level test and enhance chip testability. A 1-Kb on-chip self-test program includes a software key for data security in the system level test. 2 refs.

Descriptors: COMPUTERS, MICROCOMPUTER; DATA STORAGE, DIGITAL--Fixed; DATA PROCESSING--Security of Data; **INTEGRATED CIRCUITS** --Modular Construction

Identifiers: ERASABLE PROGRAMMING **READ ONLY MEMORY (EPROM)**; **ELECTRICALLY EPROM (EEPROM)**; SECURITY-CHECK CIRCUITS; MODULE-LEVEL TEST ; ON-CHIP SELF-TEST

Classification Codes:

722 (Computer Hardware)

72 (COMPUTERS & DATA PROCESSING)

17/5/14 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

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03722737 INSPEC Abstract Number: B90060369, C90063467

Title: **ROM and RAM blocks a la carte**

Author(s): Lauxen, B.

Journal: Elektronik Journal vol.24, no.13-14 p.38,41

Publication Date: 21 July 1989 Country of Publication: West Germany

CODEN: EKTJAY ISSN: 0013-5674

Language: German Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: Describes and explains the Toshiba module generator, used for automatic production of the simulation and mask **data** for **RAM** and **ROM** ASICs of the sea of gates and standard cells types. The design process is shown in a diagram. Simulation models with time parameters dependent on the configuration are given out in Toshiba standard network description language. The **data** for the mask, **obtained** by the tile method, are in the form of horizontally and vertically arranged sheet cells. It is expected that further development will allow the module generator to be employed in the design of programmable logic arrays. (0 Refs)

Subfile: B C

Descriptors: application specific **integrated circuits**; cellular arrays; logic arrays; logic CAD; random-access storage; read-only storage

Identifiers: Toshiba module generator; mask data; **RAM**; **ROM**; ASICs; sea of gates; standard cells types; time parameters; standard network description language; tile method; sheet cells; programmable logic arrays

Class Codes: B1265B (Logic circuits); C5210B (Computer-aided logic design); C5120 (Logic and switching circuits)

17/5/25 (Item 1 from file: 94)

DIALOG(R)File 94:JICST-EPlus

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04112443 JICST ACCESSION NUMBER: 99A0412448 FILE SEGMENT: JICST-E

Features and Applications of **FeRAM**.

TOYOSHIMA H (1); KOBATAKE H (1)

(1) Nec Corp.

NEC Res Dev, 1999, VOL.40,NO.2, PAGE.206-209, FIG.5, REF.14

JOURNAL NUMBER: G0138AAA ISSN NO: 0547-051X CODEN: NECRA
UNIVERSAL DECIMAL CLASSIFICATION: 537.226.4 621.382.2/.3.049.77 681.327
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication

ABSTRACT: Ferroelectric random access memory (FeRAM) offers nonvolatile data storage, low-voltage operation, and fast write speeds. The fundamental FeRAM structure and operations are reviewed. The features of FeRAM are compared with those of conventional memories and shown to be attractive for many types of portable electronic devices. (author abst.)

DESCRIPTORS: ferroelectrics; RAM; smart card; thin film condenser; MISFET; high density packaging; hysteresis; polarization reversal; electric power consumption; nonvolatile memory; CMOS structure; durability

IDENTIFIERS: FeRAM; packaging density

BROADER DESCRIPTORS: dielectrics; dielectric material; material; memory(computer); equipment; card(sheet); condenser(capacitor); circuit component; parts; FET; transistor; semiconductor device; solid state device; packaging(mounting); irreversible process; process; electrical property; reversal; energy consumption; consumption; MOS structure; device structure; resistance(endure)

CLASSIFICATION CODE(S): BM05030B; NC03162T; JC04060F

17/5/28 (Item 3 from file: 6)

DIALOG(R)File 6:NTIS

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0464390 NTIS Accession Number: DP-1351/XAB

A Desk-Top Microcomputer

Byrd, J. S.

Du Pont de Nemours (E.I.) and Co., Aiken, S.C. Savannah River Lab.

Corp. Source Codes: 387548

Aug 74 68p

Journal Announcement: GRAI7424

Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.

NTIS Prices: PC A04/MF A01

Contract No.: AT(07-2)-1

A low-cost desk-top microcomputer was designed and fabricated using an Intel Model 8008 central processor module. Programs can be sequentially loaded into a 2K x 8-bit random access memory with an octal data entry keyboard. Other key operations include single point and sequential data readout, clear data entry, program interrupt, and program single cycle operation. Programs can be permanently stored in a 1K x 8-bit programmable read - only memory. All circuits were realized with plug-in dual in-line integrated circuit modules and wire-wrap connections. This paper discusses applications of the microcomputer as a training aid and for process control. (Modified author abstract)

Descriptors: *Microcomputers; *Logic design

Identifiers: NTISAEC

Section Headings: 62A* (Computers, Control, and Information Theory--Computer Hardware)

17/5/31 (Item 1 from file: 583)

DIALOG(R)File 583:Gale Group Globalbase(TM)
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06067027

AVS introduces Bull CP8 **smart card** for Thai banks

THAILAND: AVS LAUNCHES BULL CP8 **SMART CARD** HERE

Bangkok Post (XBN) 26 Oct. 1994 P.5 Post Database

Language: ENGLISH

In Thailand, Advance Vision Systems (AVS) Co, a distributor of Bull CP8 Co, has launched a Bull CP8 microcomputer card in the country, targeted specifically at local banks to replace all existing cards used today. The **smart card** comes with a microcomputer chip with a 2-64 KB **RAM** and **ROM** for **accessing data**, a picture, a finger print and a signature of the owner. It also meets up the ISO 7816 standard. The card can be used as a credit card/debit card and doubles up as a **electronic purse**. Each card costs between B 100 to B 1,000 depending on its memory.

COMPANY: BULL CP8; AVS; ADVANCE VISION SYSTEMS

PRODUCT: Debit Card Svcs (6020DC); Nonbank Credit Card Firms (6141);

Smart Cards (3078SC);

EVENT: Marketing Procedures (24);

COUNTRY: Thailand (9THA);

21/5/2 (Item 2 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
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03476002 E.I. Monthly No: EI9209115826

Title: Smart solutions.

Author: Bright, Julian

Source: Telecommunications v 26 n 2 Feb 1992 p 30, 75-76

Publication Year: 1992

CODEN: TLCOAY **ISSN:** 0040-2494

Language: English

Document Type: JA; (Journal Article) **Treatment:** A; (Applications)

Journal Announcement: 9209

Abstract: The modern **smart card** is the size of a plastic credit card, and consists of an electronic **memory** or microprocessor device embedded into a plastic card. **Smart cards** have much greater security, information storage, and processing capacity than the familiar magnetic strip card. Two basic types of **smart cards** are currently in use; **memory** cards and microprocessor cards. **Memory** cards can offer read and write **memory** protection, and can be used with a personal identification number (PIN) for added security. When used in portable **file** applications, free **memory access** allows the **content** to be modified and updated as required. Microprocessor cards offer secure information management and processing, with data protection and encryption functions. Use of electrically erasable programmable **read - only memory (EEPROM)** devices can additionally offer reusable **memory** capability for applications where security information or data may need to be updated, as with rechargeable prepaid cards, secure portable data **files**, logical **access** control, and TV subscriber cards.

Descriptors: MICROPROCESSOR CHIPS--* **Smart Cards**; DATA STORAGE, DIGITAL; DATA STORAGE--Security of Data; DATA PROCESSING--Security of Data

Identifiers: PLASTIC CARDS; **EEPROM**

Classification Codes:

722 (Computer Hardware); 723 (Computer Software); 911 (Industrial Economics)

72 (COMPUTERS & DATA PROCESSING); 91 (ENGINEERING MANAGEMENT)

21/5/4 (Item 2 from file: 2)
DIALOG(R)File 2: INSPEC
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03266638 INSPEC Abstract Number: C89003918, D89000047

Title: The Active Smartcard-the future travellers' companion?

Author(s): Ruckwood, R.

Conference Title: SMART CARD '88: International Conference and Workshop on Smart Card Applications and Technologies p.12 pp.

Publisher: PLF Commun, Peterborough, UK

Publication Date: 1988 **Country of Publication:** UK 3 vol. (222+174+44) pp.

Conference Date: 20-22 June 1988 **Conference Location:** London, UK

Language: English **Document Type:** Conference Paper (PA)

Treatment: Practical (P); Product Review (R)

Abstract: The Thomas Cook prototype Active Smartcard is a customised version of Smartcard International Inc's Ulticard. This is a 3 mm thick card with the centre-left standard contact position. The card contains a Card Operating System (COS) in **ROM**. This manages all communication via the contact area. Using COS functions the application code can selectively grant or deny **access** to card **files**, grant or deny use of instructions from the POS device, and force the card and POS device to authenticate each

other. The facilities provided on the card are as follows: payment and transaction recording services; profile information services; authentication for special services; itinerary and related information services; and utility services. (0 Refs)

Subfile: C D

Descriptors: **smart cards**

Identifiers: Active Smartcard; Thomas Cook prototype; Ulticard; Card Operating System; ROM ; application code; card files; POS device; payment; transaction recording; profile information services; itinerary; utility services

Class Codes: C7120 (Finance); D2050E (Banking)

21/5/5 (Item 1 from file: 99)

DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

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1396731 H.W. WILSON RECORD NUMBER: BAST96061174

Smart - card OSs aid application development

Nath, N. S. Manju;

EDN v. 41 (Oct. 10 '96) p. 22+

DOCUMENT TYPE: Product Evaluation ISSN: 0012-7515 LANGUAGE: English

RECORD STATUS: Corrected or revised record

ABSTRACT: **Smart - card** operating systems (OSs) provide the common platform that card vendors and application developers require to design and develop applications. A **smart - card** OS and a computer OS are different in that the **smart - card** OS has to control only one piece of hardware, namely, the data-storage **EEPROM** . In addition, the **smart - card** OS is fixed in the ROM of the **smart - card** microprocessor and cannot be expanded. A **smart - card** OS provides operations that a computer OS does not provide, including access control and file management with the **EEPROM** . **Smart - card** OS information can be obtained by designers via the Internet.

DESCRIPTORS: **Smart cards** ; Computer operating systems; Product evaluation;

21/5/6 (Item 1 from file: 583)

DIALOG(R)File 583:Gale Group Globalbase(TM)

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04216797

SMART - CARD BASED SECURITY SYSTEM

US - **SMART - CARD** BASED SECURITY SYSTEM

Defense Electronics (DFE) 0 April 1991 p59

Personal Computer Card (Lakeland, FL), has a PC security system using a **smart card** read by a mini-reader attached to a computer. The 8-bit micro **smart card** can be programmed to give varying levels of access to the PC and has 2 Kbyte **memory** . It stores passwords and gives an audit trail of **accessed files** . Prices start at USD149.*

PRODUCT: **Smart Cards** (3078SC); Computer & Data Security Software (7372CD); CAD/CAM Mechanical Software (COSW);

EVENT: PRODUCTS, PROCESSES & SERVICES (30);

COUNTRY: United States (1USA); NATO Countries (420); South East Asia Treaty Organisation (913);

21/5/7 (Item 2 from file: 583)
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03024030

DEVELOPMENTS IN SMART CARDS

UK - DEVELOPMENTS IN SMART CARDS

Electronics Weekly (ECW) 1 November 1989 p19
ISSN: 0013-5224

Gemplus Card International (France) is proposing a chip operating system (COS) for smart cards as the industry standard. The memory of the smart card is organised as files of various lengths and the COS assigns an area number to each file. In this way information can only be accessed from a permitted file. An issuer of a smart card can therefore sell part of the memory to other companies each offering a range of pre-paid services. Midland Bank (UK) and Barclays Bank (UK) are testing the feasibility of hiring out parts of their cards to other organisations, with the Darlington Leisure Centre issuing pre-paid Barclaycards for visitors to spend on the premises. Gemplus is producing cards for Sky, a satellite TV company, for use by Sky customers wishing to access Sky Movies and The Disney Channel. Logicam (France) is offering Telecam which allows access to a mainframe computer using a specially encrypted card inserted into a controller, to reduce fraudulent access through personal computers and wide area networks.

PRODUCT: Smart Cards (3078SC);

EVENT: MARKET & INDUSTRY NEWS (60);

COUNTRY: United Kingdom (4UK); OECD Europe (415); NATO Countries (420);
South East Asia Treaty Organisation (913);

24/5/2 (Item 2 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
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05384253 E.I. No: EIP99104824129

Title: Practical security systems with smartcards
Author: Itoi, Naomaru; Honeyman, Peter
Corporate Source: Univ of Michigan, Ann Arbor, MI, USA
Conference Title: Proceedings of the 1999 7th Workshop on Hot Topics in Operating Systems (HotOS-VII)
Conference Location: Rio Rico, AZ, USA **Conference Date:** 19990329-19990330
Sponsor: IEEE-TCOS; AT and T; Compaq Corporation; HP Labs; et al.
E.I. Conference No.: 55660
Source: Proceedings of the Workshop on Hot Topics in Operating Systems - HOTOS 1999. p 185-190
Publication Year: 1999
CODEN: 002082
Language: English
Document Type: JA; (Journal Article) **Treatment:** T; (Theoretical)
Journal Announcement: 9911W3
Abstract: Secure hardware is a useful tool for enhancing computer system security. Traditionally, researchers have attempted to build secure operating systems by creating secure hardware and developing on top of it. Our approach is to integrate commodity secure hardware, i.e., smartcards, into existing operating systems. This paper describes three projects aimed at practical secure operating systems based on smartcards: smartcard integration with Kerberos V5, a UNIX filesystem for smartcards, and Internet Protocol on smartcards. The first two are implemented and indicate satisfactory performance, while the last is under development. (Author abstract) 18 Refs.
Descriptors: Smart cards ; UNIX; Internet; Network protocols; Security of data; Response time (computer systems); Computer systems programming; Management information systems
Identifiers: File systems ; Internet protocol (IP)
Classification Codes:
722.4 (Digital Computers & Systems); 723.2 (Data Processing); 723.1 (Computer Programming)
722 (Computer Hardware); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

24/5/7 (Item 7 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
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04063896 E.I. No: EIP95022562212

Title: Microsoft flash file system
Author: Torelli, Peter
Corporate Source: Rensselaer Polytechnic Inst
Source: Dr. Dobb's Journal of Software Tools for Professional Programmer v 20 n 2 Febr 1995. p 62
Publication Year: 1995
CODEN: DDJTEQ **ISSN:** 1044-789X
Language: English
Document Type: JA; (Journal Article) **Treatment:** G; (General Review)
Journal Announcement: 9504W3
Abstract: The first FFS implementation did not function smoothly: FEDE chains grew out of control, reclaim would occur at the wrong moments. In the present implementation of FFS by SystemSoft and Microsoft these issues are addressed. It is shown that FFS can achieve reasonable performance.

Furthermore, competition between FTL and FFS approaches has caught the attention of systems designers. Finally, the procedures presented in this article cover the basic mechanics for the purpose of letting the user to format a card, follow FEDE chains, add **files** or **directories** and so on.

Descriptors: Database systems; File organization; DOS; Data structures; Data storage equipment; **Smart cards** ; User interfaces; Computer simulation; Hierarchical systems; Storage allocation (computer)

Identifiers: Flash **file system** ; File allocation table; **File** entry **directory** entry list; Block allocation members; File name

Classification Codes:

723.3 (Database Systems); 723.2 (Data Processing); 723.1 (Computer Programming); 722.1 (Data Storage, Equipment & Techniques); 722.2 (Computer Peripheral Equipment); 723.5 (Computer Applications)

723 (Computer Software); 722 (Computer Hardware)

72 (COMPUTERS & DATA PROCESSING)

24/5/8 (Item 1 from file: 2)

DIALOG(R)File 2:INSPEC

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6806561 INSPEC Abstract Number: C2001-02-7140-060

Title: Implementing FISC IC card specification and developing health care application using Java Card

Author(s): Tien-Yan Ma; Ting-Wei Hou

Author Affiliation: Dept. of Eng. Sci., Nat. Cheng Kung Univ., Tainan, Taiwan

Conference Title: Proceedings International Symposium on Multimedia Software Engineering p.184-90

Publisher: IEEE Comput. Soc, Los Alamitos, CA, USA

Publication Date: 2000 Country of Publication: USA xiii+446 pp.

ISBN: 0 7695 0933 9 Material Identity Number: XX-2000-03057

U.S. Copyright Clearance Center Code: 0 7695 0933 9/2000/\$10.00

Conference Title: Proceedings International Symposium on Multimedia Software Engineering

Conference Sponsor: IEEE Comput. Soc.; Tamkang Univ.; Taiwan Ministr. Educ.; Taiwan Nat. Sci. Council

Conference Date: 11-13 Dec. 2000 Conference Location: Taipei, Taiwan

Language: English Document Type: Conference Paper (PA)

Treatment: Applications (A); Practical (P)

Abstract: The Java Card specification extends Java technology into **smart cards** . The FISC (Financial Information Service Co., Ltd.) IC card specification is the only financial **smart card** standard in Taiwan. In the Peng-Hu Health Care IC Card Project, we adopted FISC-compatible IC cards. In this paper, we describe an approach to develop a FISC-compatible application, based on the health care **file system** , using the Java Card specification. A shareable interface is defined to share the FISC **file system** with applets on the same card. (11 Refs)

Subfile: C

Descriptors: financial data processing; health care; Java; medical information systems; **smart cards** ; standards

Identifiers: FISC IC card specification; Java Card specification; financial **smart card** standard; Financial Information Service Co.; Peng-Hu Health Care IC Card Project; integrated circuit cards; health care **file system** ; shareable interface; FISC **file system** ; applets; health information system; financial information system

Class Codes: C7140 (Medical administration); C6110J (Object-oriented programming); C6140D (High level languages); C7120 (Financial computing)

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24/5/9 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC
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6522406 INSPEC Abstract Number: C2000-04-7120-035

Title: Biometrics electronic purse

Author(s): Wahab, A.; Tan, E.C.; Heng, S.M.

Author Affiliation: Div. of Comput. Syst., Nanyang Technol. Univ., Singapore

Conference Title: Proceedings of IEEE. IEEE Region 10 Conference. TENCON 99. 'Multimedia Technology for Asia-Pacific Information Infrastructure' (Cat. No.99CH37030) Part vol.2 p.958-61 vol.2

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 1999 Country of Publication: USA 2 vol.xxxvii+1583 pp.

ISBN: 0 7803 5739 6 Material Identity Number: XX-2000-00029

U.S. Copyright Clearance Center Code: 0 7803 5739 6/99/\$10.00

Conference Title: Proceedings of IEEE. IEEE Region 10 Conference. TENCON 99. 'Multimedia Technology for Asia-Pacific Information Infrastructure'

Conference Sponsor: Inst. Electron Eng. Korea; Korea Inf. Sci. Soc.; Korean Inst. Electr. Eng.; Korean Inst. Commun. Sci.; IEEE Region 10; Minist. Sci. & Technol.; Minist. Educ.; Cheju Province

Conference Date: 15-17 Sept. 1999 Conference Location: Cheju Island, South Korea

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: This paper proposes an efficient and universal **smart card** system to be implemented for banking applications over the Internet to support the fast growing electronic commerce industry. Encryption technology such as digital certificates and signatures were exploited and integrated with other authentication specifications (e.g. SET) to provide secure transactions over a distributed network. A simple PIN code verification is no longer sufficient and would require a more complex and fool proof authentication method. A 56-bit DES encryption algorithm can easily be broken in just 2 to 3 days using the EFF DES CRACKER, an unclassified ASIC machine. This paper looks into using biometrics as a means of authentication, thus requiring a new generation of **smart card** technology to be implemented in banking and a multiple applications environment. A prototype of the proposed biometrics electronic purse (BEP) was built using the Schlumberger Cyberflex Multi8K Java Card with simple **file management** utilities software to upload/download biometrics template to/from the Java card. (7 Refs)

Subfile: C

Descriptors: bank data processing; biometrics (access control); cryptography; electronic money; Internet; Java; message authentication; **smart cards**

Identifiers: biometrics; electronic purse; **smart card**; banking applications; Internet; electronic commerce; encryption; digital certificates; digital signatures; authentication specifications; secure transactions; DES encryption algorithm; EFF DES CRACKER; Cyberflex Multi8K Java Card; **file management**

Class Codes: C7120 (Financial computing); C1260C (Cryptography theory); C6130S (Data security); C7210N (Information networks)

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24/5/10 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC
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6055559 INSPEC Abstract Number: B9812-7540-001, C9812-7140-003

Title: Development and present state of the medical information system. 2. R&D and verification experimentation of the integrated system

Author(s): Futamura, K.

Journal: JIPDEC Informatization Quarterly no.112 p.29-36

Publisher: Japan Inf. Processing Dev. Center,

Publication Date: 1998 Country of Publication: Japan

CODEN: JIQUET ISSN: 1340-3346

SICI: 1340-3346(1998)112L:29:DPSM;1-C

Material Identity Number: B371-98002

Language: English Document Type: Journal Paper (JP)

Treatment: Practical (P); Experimental (X)

Abstract: For part 1, see *ibid.*, no. 112, pp. 13-28 (1998). The original copies of medical images used in medical practice could be stored on an electronic medium, such as a magneto-optical disk, instead of on conventional X-ray films. There is also an attempt to make use of card media, such as IC cards that are input with health and medical information for each individual to keep and manage, in medical practice at medical care organizations and in health consultations and for guidance at health centers. In addition, along with the popularization of networks, represented by the Internet, patient information and medical images are being transmitted and linked by telecommunications, for the realization of telemedicine. In order to integrate the magneto-optical disk, IC card and telecommunications for use, we developed integrated software for the base of security communication, together with the use of an existing **file manager** (FM) and contents access manager (CAM), and conducted verification experiments. As a result, we were able to ensure full security from integrated software, realizing the reliable authorization of communicating persons, protection of privacy with ciphering, and detection of alterations. (0 Refs)

Subfile: B C

Descriptors: biomedical engineering; cryptography; data privacy; health care; integrated software; Internet; magneto-optical recording; medical image processing; medical information systems; program verification; **smart cards**; visual databases

Identifiers: medical information system; R&D; research and development; verification experimentation; integrated system; medical images; magneto-optical disk; IC card media; health information; medical care organizations; health consultations; health centers; Internet; patient information; telecommunications; telemedicine; integrated software; security communication; **file manager**; contents access manager; reliable authorization; privacy protection; ciphering; alteration detection; Japan

Class Codes: B7540 (Hospital Engineering); B4120 (Optical storage and retrieval); B3120B (Magnetic recording); B4160 (Magneto-optical devices); B6210L (Computer communications); B6120B (Codes); C7140 (Medical administration); C5320C (Storage on moving magnetic media); C5320K (Optical storage); C5620W (Other computer networks); C6160S (Spatial and pictorial databases); C6130S (Data security)

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24/5/11 (Item 4 from file: 2)

DIALOG(R)File 2:INSPEC

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4886505 INSPEC Abstract Number: C9504-6130S-008

Title: Key management in an encrypting file system

Author(s): Blaze, M.

Author Affiliation: AT&T Bell Labs., USA

Conference Title: Proceedings of the Summer 1994 USENIX Conference p.
27-35

Publisher: USENIX Assoc, Berkeley, CA, USA

Publication Date: 1994 Country of Publication: USA 316 pp.

Conference Title: Proceedings of the Summer 1994 USENIX Conference

Conference Date: 6-10 June 1994 Conference Location: Boston, MA, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: As distributed computing systems grow in size, complexity and variety of application, the problem of protecting sensitive data from unauthorized disclosure and tampering becomes increasingly important. Cryptographic techniques can play an important role in protecting communication links and file data, since access to data can be limited to those who hold the proper key. In the case of file data, however, the routine use of encryption facilities often places the organizational requirements of information security in opposition to those of information management. Since strong encryption implies that only the holders of the cryptographic key have access to the cleartext data, an organization may be denied the use of its own critical business records if the key used to encrypt these records becomes unavailable (e.g., through the accidental death of the key holder). This paper describes a system, based on cryptographic "smartcards," for the temporary "escrow" of file encryption keys for critical files in a cryptographic **file system**. Unlike conventional escrow schemes, this system is bilaterally auditable, in that the holder of an escrowed key can verify that, in fact, he or she holds the key to a particular directory and the owner of the key can verify, when the escrow period is ended, that the escrow agent has neither used the key nor can use it in the future. We describe a new algorithm, based on the DES cipher, for the online encryption of file data in a secure and efficient manner that is suitable for use in a smartcard. (14 Refs)

Subfile: C

Descriptors: cryptography; file organisation; **smart cards**

Identifiers: distributed computing systems; unauthorized disclosure; tampering; cryptographic techniques; communication links; information security; information management; cryptographic key; cleartext data; smartcards; escrow schemes; DES cipher; online encryption

Class Codes: C6130S (Data security); C6120 (File organisation)

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24/5/12 (Item 5 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

4862720 INSPEC Abstract Number: C9503-6150J-004

Title: New directions for integrated circuit cards operating systems

Author(s): Paradinas, P.; Vandewalle, J.-J.

Author Affiliation: Recherche et Developpement Dossier Portable, CHRU Calmette, Lille, France

Journal: Operating Systems Review vol.29, no.1 p.56-61

Publication Date: Jan. 1995 Country of Publication: USA

CODEN: OSRED8 ISSN: 0163-5980

Language: English Document Type: Journal Paper (JP)

Treatment: General, Review (G)

Abstract: Integrated circuit cards or **smart cards** are now well-known. Applications such as electronic purses (cash units stored in cards), subscriber identification cards used in cellular telephone or access keys for pay-TV and information highways emerge in many places with millions of users. More services are required by applications providers and card holders. Mainly, new integrated circuit cards evolve towards non-predefined multi-purpose, open and multi-user applications. Today, operating systems

implemented into integrated circuit cards cannot respond to these new trends. They have evolved from simple operating systems defining an hardware abstraction level up to **file management** systems or database management systems where the card behavior was defined once at the manufacturing level or by the card issuer. The needs for open and flexible card life cycle enabling to accommodate executable code loaded by different service providers require a new generation of **smart cards**. Operating systems based on object-oriented technologies are key components for future integrated circuit cards applications. (9 Refs)

Subfile: C

Descriptors: object-oriented methods; operating systems (computers); **smart cards**

Identifiers: integrated circuit cards operating systems; **smart cards**; electronic purses; subscriber identification cards; cellular telephone; access keys; pay-TV; information highways; applications providers; card holders; hardware abstraction level; **file management** systems; database management systems; flexible card life cycle; executable code; object-oriented technologies

Class Codes: C6150J (Operating systems); C6110J (Object-oriented programming)

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24/5/13 (Item 6 from file: 2)

DIALOG(R)File 2:INSPEC

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04128186 INSPEC Abstract Number: C9205-6130S-038

Title: **A new high-security, multi-application smart card jointly developed by Bull and Philips**

Author(s): Schnabel, P.

Conference Title: Smart Card 2000. Selected Papers from the Second International Smart Card 2000 Conference p.9-15

Editor(s): Chaum, D.

Publisher: North-Holland, Amsterdam, Netherlands

Publication Date: 1991 Country of Publication: Netherlands xi+206 pp.

ISBN: 0 444 89266 4

Conference Date: 4-6 Oct. 1989 Conference Location: Amsterdam, Netherlands

Language: English Document Type: Conference Paper (PA).

Treatment: Practical (P)

Abstract: Bull and Philips, two major companies involved in **smart card** development decided to join their efforts and their know-how and created a common development team aiming to design and implement a high-security, multi-application card operating system. It has the following characteristics: **file management** functions for hierarchical file structures; flexible data management facilities, allowing extensive customization of data protection and logical data access; possibility to host different algorithms to be used by the cryptographic functions supported by the card; implementation of a set of generic commands in accordance with the work in progress at ISO; portability to allow adaptation to different components; and open design in order to permit creation of a product line with different characteristics depending on the available resources, and upward compatibility between its members. (0 Refs)

Subfile: C

Descriptors: cryptography; file organisation; security of data; **smart cards**

Identifiers: standards; multi-application **smart card**; Bull; Philips; **file management** functions; flexible data management; data protection;

logical data access; cryptographic functions; ISO
Class Codes: C6130S (Data security)

24/5/14 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC
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03287315 INSPEC Abstract Number: C89008666

Title: Into a 3rd generation-the 'active' card
Author(s): Bright, R.
Author Affiliation: Smart Card Int., Orpington, UK
Conference Title: SMART CARD '88: International Conference and Workshop on Smart Card Applications and Technologies p.6 pp.
Publisher: PLF Commun, Peterborough, UK
Publication Date: 1988 **Country of Publication:** UK 3 vol. (222+174+44) pp.

Conference Date: 20-22 June 1988 **Conference Location:** London, UK
Language: English **Document Type:** Conference Paper (PA)
Treatment: Practical (P); Product Review (R)
Abstract: SCI's ULTICARD and its compatible 'passive' card-the MAGNACARD-are at the leading edge of **smart card** technology thanks to the advanced software, **file management** and chip design common to both products. Over the years, many industry commentators have criticised the limited choice and functionalities which, due largely to the absence of suitable technology, unavoidably constrained the potential opportunities envisaged for **smart cards**. With the advent of the ULTICARD, in particular, most of these objections have been removed and the way has been opened to exploit its unique features in an unparalleled range of multiple applications as, indeed, the recent decision by Thomas Cook to develop a combined business travel and financial services solution amply demonstrates. There is now strong evidence that this initiative will be quickly followed by other organisations as the realisation spreads that active cards now offer the equivalent of a 'personal computer in the pocket'. (0 Refs)

Subfile: C
Descriptors: financial data processing; **smart cards**; travel industry
Identifiers: passive card; pocket computers; ULTICARD; MAGNACARD; **smart card**; **file management**; chip design; business travel; financial services; active cards
Class Codes: C7100 (Business and administration)

24/5/15 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC
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03287058 INSPEC Abstract Number: C89008132

Title: Security-securacces experience
Author(s): Tapie, A.
Author Affiliation: Caisse Nat. d'Assurance Vieillesse, Paris, France
Conference Title: SECURICOM 88: 6th Worldwide Congress on Computer and Communications Security and Protection p.77-90
Publisher: SEDEP, Paris, France
Publication Date: 1988 **Country of Publication:** France 404 pp.
Conference Sponsor: Agence Protection Programmes; Alarmes Protection Securite; et al
Conference Date: 15-17 March 1988 **Conference Location:** Paris, France
Language: French **Document Type:** Conference Paper (PA)
Treatment: Practical (P)

Abstract: Shows the solutions taken by CNAVTS, national organism of social security, to secure the access to the nominative **files**. Inside a security **director** plan, the experience of securacces (security software running on French computer BULL DPS 7) demonstrates the feasibility of a generalized access control using a microprocessor card (CP8) from every where by all workstations (terminal, microcomputer, minitel). (0 Refs)

Subfile: C

Descriptors: file organisation; security of data; **smart cards**

Identifiers: CNAVTS; national organism of social security; nominative files; security director plan; securacces; security software; French computer; BULL DPS 7; access control; microprocessor card; CP8; workstations; terminal; microcomputer; minitel

Class Codes: C6130 (Data handling techniques); C6120 (File organisation)
)

24/5/16 (Item 9 from file: 2)

DIALOG(R)File 2:INSPEC

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02264606 INSPEC Abstract Number: D84001463

Title: Controlling the flow (insurance industry)

Author(s): Mortenson, P.K.

Journal: Best's Review - Property/Casualty Insurance Edition vol.85,
no.1 p.74-6

Publication Date: May 1984 Country of Publication: USA

CODEN: BRPIDU ISSN: 0161-7745

Language: English Document Type: Journal Paper (JP)

Treatment: General, Review (G); Practical (P)

Abstract: Information sharing among insurance companies is one way in which a company can use information distribution to improve its 'bottom line'. Another promising method is agency automation. Once an agency has a computer, information can travel quickly between the agency and the home office via one of several communication networks. New technology continues to bring profound changes in the insurance industry. One area of importance is the evolution of artificial intelligence. Nationwide is currently using a decision support system which exhibits some of the features of artificial intelligence. Another interesting development is the concept of **smart cards**, which resemble credit cards, but contain, in addition to a magnetic identity strip, an embedded programmable microprocessor. Waiting in the wings is a breakthrough in the storage and retrieval of data. Optical document **file systems**, based on erasable optical disc technology, are due to enter the market place in 1985, and 1986 should see the introduction of optical storage workstations. In choosing modern technology each insurance company is actually choosing where to enhance and where to restrict the flow of information. Successful companies will be those in which policies on information flow like policies on cash flow, are made at the highest levels. (0 Refs)

Subfile: D

Descriptors: artificial intelligence; insurance data processing; management information systems; optical storage

Identifiers: insurance agency automation; optical document **file systems**; insurance companies; information distribution; communication networks; artificial intelligence; Nationwide; decision support; **smart cards**; embedded programmable microprocessor; erasable optical disc technology; optical storage workstations; information flow

Class Codes: D2080 (Information services and database systems); D2050G (Insurance)

24/5/17 (Item 1 from file: 233)
DIALOG(R)File 233:Internet & Personal Comp. Abs.
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00600403 00IA04-007

Lose the paper

Lunt, Penny

Imaging & Document Solutions , April 1, 2000 , v9 n4 p52-61, 9 Page(s)

ISSN: 1063-4320

Languages: English

Document Type: Articles, News & Columns

Geographic Location: United States

Examines the use of electronic forms by American business. States that forms are behind 83 percent of all corporate activity. Says that companies spend \$6 billion a year on pre-printed forms and \$360 billion to process them. Adds that 30 percent of pre-printed forms become obsolete before they are used. Reports that the need for signatures has been one of the biggest hurdles preventing more widespread use of electronic forms. Notes that there is no one law governing digital signatures and that every state has its own regulations. Notes that security for digital certificates and signatures is available with **smart cards** and cryptographic tokens. Discusses system integration considerations. Surmises that e-form options must fit the current computer environment, user profile, application, and budget. States that e-form vendors include JetForm, PureEdge, Shana, Datakey, FileNet, Entrust, Verisign, and Silanis. Contains six photos and four sidebars. (sps)

Descriptors: Records Management; Document Management System; Image Processing; Forms; Digital Certificates; Image Management; **File Management**

24/5/18 (Item 2 from file: 233)
DIALOG(R)File 233:Internet & Personal Comp. Abs.
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00537173 99PI06-007

Lock up your laptop -- The IBM SmartCard Security Kit protects your notebook from prying eyes and sticky fingers

Somers, Asa

PC Magazine , June 8, 1999 , v18 n11 p49, 1 Page(s)

ISSN: 0888-8507

Company Name: IBM Corp.

URL: <http://www.ibm.com/pc/us/accessories>

Product Name: IBM SmartCard Security Kit

Languages: English

Document Type: Hardware Review

Grade (of Product Reviewed): A

Hardware/Software Compatibility: IBM PC Compatible

Geographic Location: United States

Presents a favorable review of the IBM SmartCard Security Kit (\$200, street), a PC Card-based security solution for notebook computers from IBM Corp. of Raleigh, NC (800). Explains that it is designed to block unauthorized access to sensitive data, as well as protect against laptop theft. States that its level of security cannot be compromised in the way password security can. Says that it includes a PC Card-based SmartCard reader and software suite. Calls it easy to install. Features secure-screen-saver; data encryption options for **files** , **directories** , and folders; and support for Digital Signature for access to compatible Web sites. Points out that it can only be installed on notebooks on which CD-ROM and floppy drives are available simultaneously. Concludes that

overall, this is a good, reasonably-priced solution for securing systems against information theft. Includes one photo. (kgh)

Descriptors: **Smart Cards** ; Security; PCMCIA; Encryption; Mobile Computing

Identifiers: IBM SmartCard Security Kit; IBM Corp.

24/5/19 (Item 3 from file: 233)

DIALOG(R)File 233:Internet & Personal Comp. Abs.

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00513651 98PM11-023

Dear John -- Killer apps

Somerson, Paul

PC Computing , November 1, 1998 , v11 n11 p83, 1 Page(s)

ISSN: 0899-1847

Languages: English

Document Type: Articles, News & Columns

Geographic Location: United States

PAUL SOMERSON column predicts that new ``killer applications'' are on the horizon - inventive software for home banking, improved search engines, real graphics programs, and digital speech. Describes the potential for **smart cards** to replace bill paying, credit cards, health-insurance IDs, and drivers licenses. Remarks that search engines must get smarter by grouping results and speeding up Web returns. Contends that better, simpler graphics programs will result from the growth of digital cameras. Suggest that when some larger vendors get interested, computers that list and reply will quickly be developed. Mentions the potential (MPEG-1 Audio Layer 3) players to download music, improved **file managers** , and prolific e-commerce. (amg)

Descriptors: Forecasting; Banking; Search Engines; Graphics; Digital Camera; Application Development; Speech

24/5/20 (Item 1 from file: 94)

DIALOG(R)File 94:JICST-EPlus

(c)2003 Japan Science and Tech Corp(JST). All rts. reserv.

03407794 JICST ACCESSION NUMBER: 97A0797364 FILE SEGMENT: JICST-E

Cryptographic filing system using smart card .

MORIMOTO JUNKO (1)

(1) Toshiba Corp.

Toshiba Gijutsu Kokaishu, 1997, VOL.15,NO.50, PAGE.11-13, FIG.1

JOURNAL NUMBER: L0795AAY ISSN NO: 0288-2701

UNIVERSAL DECIMAL CLASSIFICATION: 681.3.02-759

LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal

ARTICLE TYPE: Commentary

MEDIA TYPE: Printed Publication

DESCRIPTORS: card(sheet); data protection; security system; access control; cryptogram; file processing; operating system; information medium;

smart card ; file system

BROADER DESCRIPTORS: protection; system; control; treatment; system program ; computer program; software

CLASSIFICATION CODE(S): JD01020V

24/5/22 (Item 1 from file: 144)

DIALOG(R)File 144:Pascal

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14812520 PASCAL No.: 00-0494808

Secure log file download mechanisms for smart cards

Smart card research and applications : Louvain la Neuve, 14-16

September 1998

MARKANTONAKIS C

QUISQUATER Jean-Jacques, ed; SCHNEIER Bruce, ed

Information Security Group, Royal Holloway, University of London, Egham, Surrey, TW20 0EX, United Kingdom

CARDIS'98. International conference; 3 (Louvain la Neuve BEL) 1998-09-14

Journal: Lecture notes in computer science, 2000, 1820 285-304

ISBN: 3-540-67923-5 ISSN: 0302-9743 Availability: INIST-16343;

354000090100760270

No. of Refs.: 34 ref.

Document Type: P (Serial); C (Conference Proceedings) ; A (Analytic)

Country of Publication: Germany; United States

Language: English

The necessity of auditing mechanisms for smart cards is currently under thorough investigation. Both current and future real world applications impose requirements which suggest the storage of sensitive information in log files. In this paper we present various applications that demonstrate the use of audit logs, justifying their practical advantages and disadvantages. We propose computationally practical methods for creating and maintaining such log files in the light of the limited memory of smart cards. We conclude with a brief discussion of design principles for future implementations and guidelines for further research.

English Descriptors: Smart cards ; Intelligent system; Register;

Monitoring; File management ; Storage management; Smart card

French Descriptors: Carte a puce; Systeme intelligent; Registre; Monitorage ; Gestion fichier; Gestion memoire; Carte intelligente

Classification Codes: 001D02B07C

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24/5/23 (Item 1 from file: 583)

DIALOG(R)File 583:Gale Group Globalbase(TM)

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09157415

Sony To Sell Smart Card Inventory ManagementSystem

JAPAN: SMART CARD TELE- FILE SYSTEM SALE BY SONY

Nikkei Net Interactive (ATM) 06 Sep 1999 TheNikkei Industrial Daily,

p.1

Language: ENGLISH

The sale of its noncontact smart card -based Tele-File inventory management system will be embarked in Japan by Sony Corp, which is designed for video and CD rental shops. The Tele-File inventory management system comes bundled with noncontact smart cards, noncontact integrated-circuit tags, handheld reader/writer and dedicated terminal. Sony is selling the reader/writer for v 220,000 that can hold 64,000 items data with the firm's Memory Stick, while the terminal will cost v 80,000. The IC tags append to articles and books, while the smart cards are used to identify users.